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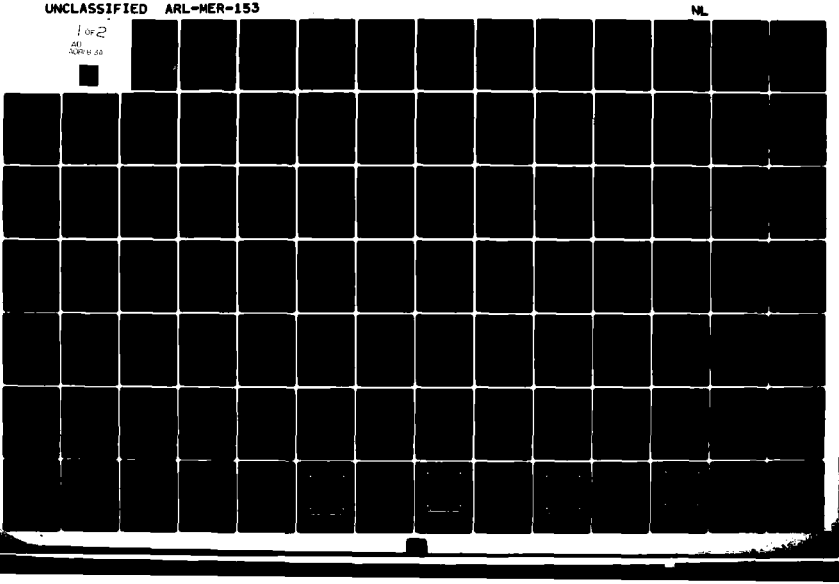

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AIRBORNE DATA PROCESSOR

by

K. F. FRASER and U. R. KRIESER

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SUMMARY

Airborne equipment developed for use in the acquisition and recording of both analogue and digital data is described. These data are recorded using a single analogue magnetic tape transport.

A reference frequency, for use in servo speed control of the ground station tape reproducing machine, is combined with speech using a balanced modulator. Recording of these data is performed using direct techniques.

Up to eight channels of analogue data, which may require measurement over large bandwidth (up to 20 kilohertz), are time multiplexed at rates which are variable over a wide range. Recording of the multiplexed data is performed using frequency modulation techniques.

A highly stable crystal oscillator generates an input clock for a time code generator which provides time-of-day in digital form.

Up to 32 channels of analogue data, requiring measurement at relatively low bandwidth but at high accuracy, are time multiplexed and converted to digital form using commercially available airborne equipment. The digital output from the above equipment together with that from the time code generator and from up to two digital transducers are multiplexed digitally. The digital data are serialized and converted to a form suitable for recording using the analogue tape machine.

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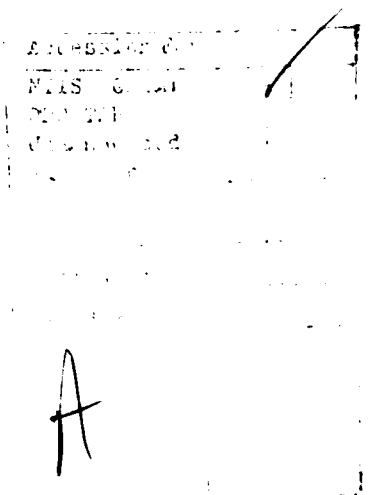

1. INTRODUCTION

This report describes a system of airborne data logging[1] adopted at the Aeronautical Research Laboratories in which the acquired data are stored on magnetic tape using a seven-track airborne analogue tape machine. Detailed analysis of the data is performed later with the aid of suitable ground station data reduction equipment.[2]

Aircraft evaluation studies involve the measurement of many physical quantities. Some quantities such as vibration displacement, noise and pressures at various points in jet engines are not normally required to be measured with extreme accuracy but frequently involve measurement over large bandwidths. Such data may be recorded using analogue techniques. Other quantities such as airspeed, altitude, air temperature and engine speed frequently have to be measured with high precision but usually over a relatively small bandwidth. High precision is required to enable basic computed quantities such as Mach Number and True Air Speed to be accurately evaluated and to enable small changes in performance to be indicated. Digital techniques must be employed for the recording of such data to the desired accuracy. Fortunately, in aircraft studies, large bandwidth and high precision are very rarely required simultaneously in a given measurement.

Because of space limitations on smaller aircraft, particularly military types, a system of recording both analogue and digital information simultaneously using the same analogue tape machine has been evolved.[1]

Due to the adverse environmental conditions under which the airborne tape machine may be required to function some small tape speed variations may be introduced. For data recorded using frequency modulation (FM) techniques (the usual form of analogue recording employed) these variations show up as noise which is inseparable from the signal components. Elimination[3] of the lower frequency components of such noise is possible if a reference frequency (as per IRIG[4]) is recorded on one track and is later used for servo speed control of the magnetic tape reproducing machine. In the system[5] developed at these laboratories a reference frequency and speech are combined using a balanced modulator and the composite signal is recorded on a single track using direct techniques.

Normally one tape track is used for digital recording and one is used for direct recording as indicated above. Hence only five tracks are left for recording of data (which may involve large bandwidths) using FM techniques. Often, however, many more than five measurements are required. Such a requirement is particularly likely for vibration recording where triaxial transducer blocks are frequently employed; three measurement channels may then be required to record vibration at any point. Up to the present, where vibration measurements have been required at a number of points, mechanical switches have been employed to switch in new sets of transducers manually during a particular run or else a number of runs have been performed to assemble the required amount of data. To overcome the above limitations a system for multiplexing and recording a number of analogue data channels over a large bandwidth has been included.[6]

An airborne analogue multiplexer and analogue to digital converter has been purchased for use in a system of digital recording. The digital output from the above analogue to digital converter together with that from a time code generator[7] and those from up to two other devices (such as transducers with digital outputs) are time multiplexed and serialized in a form suitable for recording on the analogue tape machine.

Correlation between data recorded using analogue techniques and data recorded using digital techniques is an essential requirement of the data acquisition system. For instance there may be a requirement for correlating a vibration level (deduced from FM measurements) with Mach Number (computed from a number of parameters recorded using digital techniques). The recording of time-of-day from the time code generator provides the basic identifier which enables data reduced at different times (possibly with different equipment) to be correlated in time.

Ground loop noise voltages can seriously affect the accuracy of aircraft measurements unless special precautions are taken. The problem becomes particularly severe when the acquisition equipment comprises a number of separate units (as applies in this situation). To minimize the generation of ground noise signals the DC power for the data processor (which is the subject of this paper) and also that for the multiplexer and analogue to digital converter (both these latter units are housed together) have been isolated from the aircraft supply via DC to DC converters (all units of the acquisition equipment being powered from the aircraft DC supply the negative side of which is connected to the airframe).

This report is one of a series describing equipment developed at these laboratories for use in airborne data acquisition and ground station data reduction applications.

2. GENERAL DESCRIPTION

The data processor is constructed as a single unit suitable for use in airborne applications. A block schema of the airborne data processor and associated equipment used for airborne data logging is drawn in Figure 1.

Two crystal oscillators with frequency stability better than 0·01% are employed. The frequency of the first (3·6000 MHz) is counted down to provide appropriate reference frequencies as specified by IRIG[4] for use in servo speed control of the tape reproducing machine. The frequency of the second (3·6864 MHz) is counted down and used as a master clock signal generator for use with the analogue multiplexer, the time code generator and the digital data processing circuits. Separate oscillators have been used in these two cases to ensure that the crystals are operated within the optimum range for frequency stability. If a single oscillator were used the lowest frequency which would meet both requirements (100 kHz maximum reference frequency and 40·960 kHz maximum for the digital circuits) would be 25·600 MHz.

The balanced modulator combines speech (such as flight crew commentaries) and the reference signal (switch selectable according to the tape speed used for the analogue recorder) in a form suitable for recording using a plug-in direct recording amplifier in the tape recorder.

An analogue multiplexer, which is incorporated in the data processor, is used for time multiplexing up to eight analogue signals. A wide variety of signal sampling rates may be selected via a front panel mounted switch. The sampling rate may be low compared with the lowest frequency of interest in the sampled data ("block" sampling) or, in some cases, it may be high compared with the highest frequency of interest in the sampled data ("point" sampling). Synchronization of the analogue multiplexer sampling with the time code generator enables the recorded data to be de-multiplexed at the ground station without the need for recording special synchronizing information.

Time-of-day in parallel digital form with one second resolution is provided by the time code generator. An associated time display (Fig. 1), available as a separate unit, enables the time to be displayed. Front panel mounted switches on the data processor allow the time to be set. Normally the time display is not used in flight.

The following parallel digital signals are time multiplexed by the digital multiplexer (Fig. 1) to provide a 16-line output:

(i) output (16-line) of the airborne analogue to digital converter which, with the associated analogue multiplexer, allows time multiplexing of up to 32 channels of data;
(ii) internally generated time-of-day signal (20-line) from the time code generator;
(iii) fixed data (27-line) comprising run number, day-of-the-month and month-of-the-year information (all of which are preset using front panel mounted thumbwheel switches);
(iv) output (16-line) of digital transducer No. 1;
(v) output (16-line) of digital transducer No. 2.

Serialization of the parallel output from the digital multiplexer together with the generation of appropriate synchronizing information is provided by the parallel to serial converter (Fig. 1). Control of the digital multiplexer, the analogue to digital converter and associated analogue multiplexer (Dynamics Systems Electronics Model 480001), and the parallel to serial converter is achieved using the programmer (Fig. 1) which derives timing signals from the master clock signal generator.

Specially developed plug-in digital recording amplifiers[8] enable the serialized digital output

signals from the data processor to be recorded with the analogue tape machine in either non-return-to-zero-mark (NRZM) or return-to-zero (RZ) form.

Regulated supplies of +5 V, +15 V and −15 V are required for the data processor circuits. These supplies are derived from the output of a DC to DC converter powered from the aircraft 27·5 V DC supply. With this configuration, isolation (at least at 'the power source end') between the input supply ground and the data processor common is achieved.

With the exception of the DC to DC converter, all circuits within the data processor are mounted on plug-in printed circuit boards. The DC to DC converter is mounted on a sub-chassis and is fitted with suitable power input and output connectors which enable this unit to be removed without the need for any desoldering.

Each of the blocks within the data processor of Figure 1 will be described in detail in the following sections. Information on the system of component identification used in this paper is given in Appendix 1. In the case of circuits containing digital integrated circuits logic type symbols are used and most of the integrated circuit pin numbers are also marked. Integrated circuit wiring details given in Appendix 2 provide details of supply connections plus any other connections not marked in the logic circuits. Interwiring details for printed circuits and front panel mounted components are given in Appendix 4 and component lists are given in Appendix 3.

To assist in the location of components, particularly for servicing, component layout drawings (which include component identifiers used in the associated circuit diagram) are given for each printed circuit.

3. CRYSTAL CONTROLLED TIMING SIGNALS GENERATOR

For reasons detailed in Section 2 separate crystal oscillators are used in the generation of the reference frequency signals for tape speed control and in the generation of a master clock signal for use (after suitable frequency division) with the analogue multiplexer, the time code generator and the digital data processing circuits. Appropriate division of these crystal frequencies enables a range of timing signals to be generated.

One of the circuits used for the generation of some of these timing signals incorporates integrated circuits Q001 to Q015 and associated components on printed circuit board 0 (Fig. 2). Component layout details for board 0 are given in Figure 3. The remaining circuit used for timing signal generation incorporates integrated circuits Q101 to Q106, all inverters in Q117 except Q117D, and associated components on printed circuit board 1 (Fig. 4). Component layout details for board 1 are given in Figure 5.

3.1 Reference Frequency Signal and PDM Clock Signal Generator

A crystal controlled oscillator generates a signal of 3·600 MHz frequency which is suitably divided to provide reference frequency signals for use in servo speed control of the analogue tape reproducing machine. Six reference frequencies ranging in binary steps from 100 kHz to 3·125 kHz, as specified by IRIG[4]. are provided.

In addition the output from the 3·600 MHz crystal has its frequency divided down to provide a clock signal at 900 Hz frequency for use with pulse duration modulation (PDM) units which are external to the data processor. The PDM system has, to a large extent, been superseded by the digital recording system and is therefore not likely to be used very often.

The 3·600 MHz oscillator (Fig 2) includes a series resonant crystal Y001 and two inverters Q001A and Q001B. A third inverter Q001C acts as a buffer between the output of the crystal controlled oscillator and the input to the first frequency divider Q002. Q002 and Q003 are divide-by-12 integrated circuits composed of a divide-by-two section and a divide-by-six section which may be used independently (except when reset by an external input signal). The frequency of a signal coupled to the "A-in" terminal is divided by two at the A output, and the frequency of a signal coupled to the "BC-in" terminal is divided by six at the D output. Two divisions by six in Q002 and Q003 provide a 100 kHz (square wave) at output D of Q003. The remaining divide-by-two circuit of Q003 plus the four-bit binary counter Q004 forms a cascade of five binaries so that the other five reference frequencies (from 50 to 3·125 kHz) are generated. Each of the six reference signals is buffered (via Q005A to Q005F) before being taken via a 33 ohm resistor to the data processor front panel "REF FREQ" selector switch S12 (Appendix 3.10 and Fig. 28).

The settings of S12 to be used as a function of the speed of the magnetic tape recorder are tabulated below.

Speed of magnetic tape recorder (inch/sec)	Setting required for S12	Reference frequency selector (kHz)
60	5	100
30	4	50
15	3	25
$7\frac{1}{2}$	2	12·5
$3\frac{3}{4}$	1	6·25
$1\frac{7}{8}$	0	3·125

The reference frequency selected by S12 is returned (via printed circuit board connector pin 45b of Figure 2) to the balanced modulator (Section 4.1).

Division of the crystal frequency (3·600 MHz) by 4000 is accomplished using a cascade connection of the divide-by-two circuit forming part of Q002, three divide-by-ten circuits (decade counters) Q006, Q007 and Q008, and the divide-by-two circuit forming part of Q010. The resultant 900 Hz square wave signal is transferred from the output of buffer Q015A to pin h of the front panel input connector J609.

3.2 Master Clock Signal Generator and Frequency Dividers

The master clock signal generator incorporates another crystal oscillator which includes the series resonant crystal Y002 in a circuit configuration identical to that used for the crystal oscillator mentioned above. In this case a signal having a frequency of 3·6864 MHz is generated.

The frequency of the crystal oscillator output is successively divided by five (using part of Q010), by three (using part of Q011) and then by six (using part of Q012). An output at 40·96 kHz, the highest clocking frequency required for the digital processing circuits, is provided. Six successive divisions by two (using Q011A, Q012A, Q013A, Q013B and Q013D) allow the other digital clocking signals, ranging in octave steps from 20·48 kHz to 640 Hz, to be generated. Each of the seven clock signal outputs is buffered (via Q015F and Q014A to Q014F). Selection of the appropriate clocking rate is made using the front panel switch S11. Further information on the S11 switch position to be selected at the various recording tape speeds is given in Section 6.2.

The 5·12 kHz clock signal for the data processing circuits reaches switch S11 after two additional inversions via Q117C and Q117E (Fig. 4). The square wave signal developed at the output of Q117C forms the input to a series of frequency dividers Q101 to Q106 from which clock signals at 12 separate frequencies are derived. Eleven of these are used in conjunction with the eight channel analogue multiplexer (Section 4.2) while the twelfth provides the input (a 1 Hz square wave) for the time code generator (Section 5). In the following paragraphs the frequency dividing steps will be detailed.

The four-bit binary counter Q101 divides the frequency of the 5·12 kHz input by 16 and provides outputs at 2560, 1280, 640 and 320 Hz. Part of the four-bit binary counter Q102 is used to provide outputs at 160 and 80 Hz. Operation of the analogue multiplexer in a "point sampling" mode (Section 4.2) requires the selection of one of these six signals for multiplexer clocking.

The 80 Hz signal mentioned in the previous paragraph is divided by 50 to obtain the next lower multiplexer clock frequency of 1·6 Hz. A division by five (using part of Q103) followed by a division by ten (using Q104) provides the divisor of 50. Outputs at 0·8 and 0·4 Hz are generated using the divide-by-two sections of Q103 (decade counter) and Q105 (divide-by-12 circuit) respectively. Outputs at $\frac{2}{15}$ Hz (or 8 pulses per minute) and $\frac{1}{15}$ Hz (or 4 pulses per minute) are generated by further divisions by three and then by two using the divide-by-six

section of Q105. One of these five clock signals mentioned in this paragraph is selected for use with the analogue multiplexer in the "block sampling" mode (Section 4.2).

The 1 Hz signal which forms the input to the time code generator is produced by dividing the frequency of the 16 Hz output (D output) of Q103 by 16 using the four-bit binary counter Q106.

Reset signals from the time code generator (Section 5) are periodically transferred to the frequency dividers Q101 to Q105. However, these signals normally only synchronize the frequency dividers with the time code generator just after the equipment is switched on. Thereafter they serve only to check that the frequency dividers are properly synchronized with the time code generator. The purpose of this synchronization will be explained in Section 4.2.

4. PROCESSING CIRCUITS WITH ANALOGUE OUTPUTS FOR TAPE MACHINE

The particular reference frequency signal (Section 3.1), selected for use in servo speed control of the analogue tape reproducing machine, is recorded on the same tape track of the analogue recorder as a voice signal using direct recording techniques. The voice signal may carry comments by flight crew members or other persons. A balanced modulator performs the function of combining the two signals such that no information is lost. The modulator incorporates integrated circuits Q016, Q017 and associated components mounted on printed circuit board 0 (Fig. 2).

When the tape is reproduced at a ground station, the reference frequency signal is extracted using a suitable zero crossing detector and the speech signal is reconstituted using a balanced demodulator.

Using the data processor, eight analogue input signals may be time multiplexed as a single output signal which may be recorded (normally using FM techniques) on a single track of the tape recorder. The multiplexing is performed using printed circuit board 2 (Fig. 6) for which the component layout details are given in Figure 7. Control and synchronizing signals for the analogue multiplexer are generated by printed circuit board 1 (Fig. 4) using integrated circuits Q107 to Q116, inverter Q117D, integrated circuits Q118 and Q119, and associated components.

The balanced modulator and the analogue multiplexer will now be considered separately in more detail.

4.1 Balanced Modulator

The speech signal, which is coupled to the data processor via input connector J602 and in turn coupled to board 0 at pin 47b (Fig. 2), passes to the unity gain amplifier stage incorporating Q016. This stage has its output limited to about 8 V peak to peak to prevent overdriving of the following balanced modulator stage incorporating Q017. Overdriving must be avoided as it causes spurious "zero-crossings" to be included in the balanced modulator output and leads to capstan speed errors when the tape is reproduced.[5] A high level speech signal, nominally about 2·8 V peak to peak maximum, is required at the J602 input for adequate speech recording level. A portion of the speech signal output from the Q016 stage is taken from potentiometer R007 and applied to the balanced modulator input.

The reference frequency signal (Section 3.1) as selected by front panel switch S12 is coupled to the modulator via pin 45b, buffer Q001D and capacitor C005.

The modulator stage functions as an amplifier which may be switched rapidly between the inverting and the non-inverting modes in synchronism with the reference frequency signal. Potentiometer R008 controls the level of the inserted reference frequency "carrier" signal in the balanced modulator output and ensures that the output signal envelope amplitude does not fall below about one third of its maximum value.[5,9]

The balanced modulator output is taken to the front panel connector J603 and is subsequently coupled to a direct recording plug-in available from the analogue tape recorder.

4.2 Analogue Multiplexer

The analogue multiplexer allows eight input signals, coupled to the data processor input connector J607, to be sequentially sampled and transferred to a single output line. As the multiplexer is arranged as a differential type (both signal lines switched) one of each pair of input

signal lines may be grounded to aircraft frame. Common mode ground noise voltages are largely eliminated from the multiplexer output with the arrangement used.

Multiplexing of the analogue signals is performed using four MOS integrated circuits Q203 to Q206 as indicated in Figure 6. Each includes two double-pole, single-throw switches and appropriate TTL (transistor-transistor-logic) compatible drivers.

An operational amplifier comprising Q207 and associated components converts the two-line differential outputs from the MOS multiplexer circuits to single ended form suitable for applying to an FM recording module which may be plugged into the tape recorder electronics unit. Q207 is internally protected against a short circuit at its output, and provision is made for trimming R205 for improved common mode rejection.

The amplifier stage incorporating Q207 has unity gain. To provide 100% recording level in the associated analogue recorder the inputs coupled to J601 require to be at a level of about 1 V RMS.

Each of the 11 possible multiplexer sampling rates (Section 3.2) is determined by a signal derived from the same crystal oscillator as the 1 Hz input to the time code generator. The successive selection of each of the eight multiplexer input channels is synchronized with the time code generator in such a way that, for any particular multiplexing rate, and at any specific time as indicated by the time code generator, the channel selected is known uniquely. Thus when the tape is reproduced the eight signals can be separated and identified using a demultiplexer synchronized with the reproduced time code signal. Demultiplexing can be performed using specially developed hardware (Section 8) or a digital computer with appropriate software.

Each of the multiplexer clock signals is coupled to one input of a two-input NAND gate included in Q107, Q108 or Q109 (Fig. 4). The other input to these gates is normally held in the low state by a 220 ohm resistor (R105 to R115) to common. Application of a high level to one of these inputs via the "FM MUX RATE" front panel switch S13 results in the corresponding clock signal being transferred to the input of the binary counter Q119. Gating of the selected multiplexer clock signal is performed using Q110, Q111B, Q116C and Q116B (connected as an inverter). Q119 functions as a three-bit binary counter (first divide-by-two section unused). The output from this counter is a three-line (eight state) binary signal, and determines which of the eight analogue input signals will be gated to the tape recorder via the multiplexer.

To ensure that multiplexer channel selection is correctly synchronized with the time code generator, appropriate signals derived from the latter are applied to the reset input of counter Q119. In the following table the repetition period of the synchronizing signals coupled to board 1 (Fig. 4) is tabulated.

Repetition period of synchronizing signal coupled to board 1	Input pin on board 1 to which the synchronizing signal is connected
1 second	5b
10 second	6b
20 second	7b
1 minute	13b
2 minute	8b

Selection of the appropriate repetition period of the synchronizing signal is made concurrent with that of the multiplexer sampling rate according to the setting of front panel switch S13. The appropriate selection is accomplished in a similar manner to that of the multiplexer sampling rate using gates Q112, Q113, Q114, Q115, Q111C and Q116A. The synchronizing signal is inverted by Q117D and shaped to a short duration pulse using C105 and R104 before being coupled to the reset input of Q119.

The logic states of the five counters Q101 to Q105 from which the 11 multiplexer clock signals are derived are also checked at specific intervals in synchronization with the time code generator, again for the purpose of ensuring that the three-bit output of Q119 is correctly phased

in time. This checking is accomplished every second for counters Q101 and Q102, every ten seconds for counters Q103 and Q104 and every minute for counter Q105. The synchronizing signals (coupled respectively to pins 5b, 6b and 13b of board 1) for the counters pass respectively via inverters Q117B and Q117A, Q118B and Q118A, and Q118F before being transferred to the counter reset inputs.

Initially the synchronizing signals for counters Q101 to Q105 and Q119 set these counters in known time phasing with the time code generator but thereafter they merely serve a checking function, as each counter will then maintain correct phasing unless disturbed by a noise puls..

In the following table the selected multiplexing rate, the corresponding sample period and multiplexer synchronization details are given as a function of the setting of front panel switch S13.

Setting of switch S13	Multiplexing rate	Sample period	The start of a channel 0 sample period will coincide with the following change in the time code generator*
0	4 samples per minute	15 second	Each even minute advance of the minutes register (i.e. 2 minute repetition period)
1	8 samples per minute	7·5 second	Each 1 minute advance of the minutes register (i.e. 1 minute repetition period)
2	0·4 sample per second	2·5 second	Each even 10 second advance of the seconds register (i.e. 20 second repetition period)
3	0·8 sample per second	1·25 second	Each 10 second advance of the seconds register (i.e. 10 second reptition period)
4	1·6 samples per second	625 millisecond	As above
5	80 samples per second	12·5 millisecond	Each 1 second advance of the seconds register (i.e. 1 second repetition period)
6	160 samples per second	6·25 millisecond	As above
7	320 samples per second	3·13 millisecond	As above
8	640 samples per second	1·56 millisecond	As above
9	1280 samples per second	781 microsecond	As above
10	2560 samples per second	390 microsecond	As above

* Channel 0 may be selected at other times between the arrival of successive synchronizing pulses.

The three-line output from Q119 is decoded (Fig. 6), using inverters of Q201 and NOR gates of Q202, into the logical form required for sequential sampling of the analogue input channels designated "0" to "7" (the two input lines for each channel are designated 0A and 0B, etc., in Figure 6).

5. TIME CODE GENERATOR

A time code generator produces a 20-line digital output which provides a time-of-day signal with one second resolution. The time-of-day is expressed in hours, minutes and seconds in BCD (binary coded decimal) form. The input to the time code generator is the 1 Hz square wave signal generated on board 1 (Fig. 4).

Using processing circuits described in Section 6 the digital time code signal is multiplexed with other digital signals and converted to a serial form suitable for recording on a single track of the analogue tape recorder. Signals derived from the time code generator are also used for synchronizing the analogue multiplexer (Section 4.2) and the digital processing circuits (Section 6.2).

In Figure 8 the circuit of the time code generator (which comprises board 3) is drawn and in Figure 9 the component layout is given.

5.1 Time of Day Registers

Three registers connected in cascade count incoming clock pulses and store time-of-day in seconds, minutes and hours. Each register comprises two decade counters and appropriate feedback to limit the counting range (from 0 to 59 for the seconds and the minutes registers and from 0 to 23 for the hours register).

The 1 Hz input clock signal is gated to the first decade counter Q307 (Fig. 8) via circuits which have the capability of incrementing the indicated time (Section 5.3). Q307 and Q308 count seconds and tens of seconds respectively. When Q308 acquires a count state of six the output of NAND gate Q313B will switch high momentarily. At this instant the output of the pulse "stretcher", comprising Q313C, Q313D and associated components, will switch high also; it will remain high for a time determined by the coupling network (C305 and R306) between Q313C and Q313D. The input at pin 2 of NAND gate Q313A will be held high except when the stored count is cleared. Hence the output of Q313A will normally switch low (when the pulse stretcher output is low) thus giving rise to a pulse which resets counter Q308 to the zero count state and transfers a clock pulse to the input of the minutes counter (which includes Q309 and Q310). Stretching of the reset pulse duration ensures that all flip-flops (in the register that is being reset) have time to be properly reset before the reset pulse passes.

The minutes register is identical to that for the seconds with NAND gates of Q314 performing a function similar to that of Q313 in the latter.

The arrangement for the hours register is slightly different. Here both registers Q311 and Q312 must be reset when a count state of 24 is detected. To detect this count state one output line from each of the decade counters Q311 and Q312 is coupled to the NAND gate Q315A which constitutes part of the pulse forming circuit.

Each of the decade counters has available a four line BCD output using a 1-2-4-8 code. Since the tens decade counters in both the seconds and the minutes registers are restricted to a maximum count of five, only three of the four available output lines from each are utilized. The tens decade counter in the hours register is limited to a maximum count of two; hence only two of its four output lines are used.

The digital multiplexer (Section 6.1) accepts the 20 output lines from the decade counters. These outputs are also buffered and inverted (using Q318A to Q318F, Q317A to Q317F, Q316A to Q316F, Q301A, Q301D, Q301E and Q301F) before being coupled (via front panel connector J609) to a remotely located visual time display unit.[10]

5.2 Setting of the Time of Day Registers

The time-of-day registers may be preset to any desired time reading using front panel mounted decimal thumbwheel switches S5A to S5F. By depressing front panel mounted pushbutton switch S3, the "load" inputs of Q307 to Q312 are set low and while low the logical levels present on the four input lines to each of these registers (counters) are transferred to the register outputs.

A second front panel mounted pushbutton S4 enables the three registers to be cleared to a count state of zero regardless of the state of S5.

5.3 Fine Adjustment of Preset Time

To allow synchronization of the time code generator with some external time standard, provision has been made for fine adjustment of the indicated time. Adjustment is performed in one second steps, and accomplished by selecting either the "up" or the "down" counting mode for Q307 to Q312 via front panel mounted toggle switch S6 and then depressing pushbutton S7 (also front panel mounted). If the "up" mode is chosen, operation of S7 will cause the time count to advance by two seconds during the interval in which it would normally advance one second. Selection of the "down" mode effectively causes the omission of one count of the 1 Hz input clock.

The 1 Hz square wave input to the time code generator from Q106 (Fig. 4) triggers the monostable multivibrator Q303 once per second. The multivibrator may be triggered in time synchronization with either the positive transition (via Q301C, Q301B and Q302B) or the negative transition (via Q301C and Q302D) of the input clock signal according to whether S6 is set in the "down" or the "up" position respectively.

Depressing S7 changes the "Q" output of flip-flop Q304A from its normally low state to the high state. The "Q" output of flip-flop Q304B is normally low and will remain low until S7 is released, whereupon the output of Q304B will switch high when the next pulse from the monostable multivibrator Q303 arrives. There will be a time difference, approximately equal to the duration of the monostable multivibrator pulse, between the transition to the high state at the output of Q304B and the particular transition of the 1 Hz input clock at Q301C which initiated it.

Feedback around flip-flops Q304A and Q304B causes the outputs of both to be reset to the low state almost immediately. Appropriate gating by means of Q306B, Q306C and Q306D ensures that the short duration pulse developed at the "Q" output of Q304B is transferred to either the "count up" or the "count down" input of Q307.

When the "up" mode is selected via S6 this pulse will always appear at the "count up" input of Q307 when the normal 1 Hz signal at that input is low. Thus an extra one-second count is always added to the seconds register. Further, when the "up" mode is selected, the "count down" input of Q307 will remain high as required for correct operation.

If the "down" mode is selected the normally high signal coupled to the "count down" input of Q307 will switch low for a short duration. This low level always appears after the "count up" input has switched high under the action of the 1 Hz square wave signal. The 1 Hz signal waveform is unaffected so that the seconds register increases and then decreases by a one-second count within the duration of the pulse generated by the monostable multivibrator.

Coarse adjustment of the indicated time using switches S5A to S5F and S3, followed by fine adjustment using switches S6 and S7, allows the time to be set within 0·5 s of an external time standard.

6. PROCESSING CIRCUITS WITH DIGITAL OUTPUTS FOR TAPE MACHINE

The blocks of Figure 1 which are relevant under this title are:

(i) digital multiplexers;
(ii) programmer;
(iii) parallel to serial converter.

The general function of each of these circuits has been described briefly in Section 2. In Figure 10 a more detailed block schema of these circuits is drawn.

Four printed circuit boards are used:

(i) boards 4 and 5 (identical) for the digital multiplexers;
(ii) board 6 for the programmer;
(iii) board 7 for the parallel to serial converter.

Alternative boards (designated respectively as 7A and 7B) are available for the parallel to serial converter depending on whether serial or parallel type digital recording is to be employed.

Because considerable updating of the circuits and also of some of the requirements has occurred since the original proposal[1] was formulated the operating principles of each of the circuits will now be described in detail.

6.1 Digital Multiplexers

Digital signals which are to be recorded using the analogue tape machine are derived from the following sources:

(i) analogue to digital converter (16-line input);

(ii) digital transducers (up to two 16-line inputs);

(iii) time code generator (20-line input);

(iv) preset switches on front panel of data processor (27-line input).

Signals derived from the above sources are time multiplexed as a single 16-line output using digital multiplexers Nos 1 and 2 (Fig. 10). Digital multiplexer No. 1 is used to multiplex signals from sources (iii) and (iv) into a single 16-line output. Digital multiplexer No. 2 is used to multiplex signals from sources (i) and (ii) and the output from No. 1 multiplexer into a single 16-line output.

Each consecutive 16-line signal generated at the output of digital multiplexer No. 2 is serialized and recorded together with parity checkbits as a separate "word". One complete scan of the inputs to digital multiplexer No. 2 is recorded as a separate "frame" (or "record"). One complete scan of the inputs to digital multiplexer No. 1 takes place for every four frames of data generated. However, only one word per frame is used for recording the output of digital multiplexer No. 1.

The multiplexing sequence employed by multiplexer No. 1 for time-of-day and fixed information is indicated in the table on page 11.

The table on page 11 is an updated version of one given elsewhere.[2] Slight rearrangement of the data has been incorporated to enable easier handling by digital computers employing 16-bit words which may be readily manipulated as two 8-bit bytes.

Time-of-day as generated by the time code generator is in 1–2–4–8 binary coded decimal (BCD) form and falls within the range 00 hour 00 min 00 sec to 23 hour 59 min 59 sec. Where the full 0 to 9 decimal range is not required, the usual four bits used to code a decimal digit may be reduced (e.g. three binary digits only are required to code the most significant seconds digit having a maximum value of five). Hence seven bits are used for coding seconds, another seven for minutes and six for hours.

Decimal thumbwheels mounted on the data processor actuate switches which provide BCD outputs for use with digital multiplexer No. 1. These switches allow the run number to be set anywhere in the range 0000 to 9999 (16 bits required), month-of-the-year to be set anywhere in the range 01 to 12 (5 bits required) and day-of-the-month to be set anywhere in the range 01 to 31 (6 bits required).

The multiplexer outputs a_0 to a_{15} take on the values of the multiplexer inputs a_{0_0} to a_{15_0} during the time associated with frame 0 and similarly for frames 1, 2 and 3. For subsequent frames the sequence repeats itself for each four frames.

In each subdivision of the time-of-day and fixed data the most significant bit is situated to the left in the table on page 11 (e.g. the most significant bit of the "seconds" is a_{9_0} and the least significant bit is a_{15_0}).

To enable the time-of-day and the fixed data to be separated by ground station equipment a two-bit identifier as specified in the table on page 11 is included at the start of each word (outputs a_0 and a_1).

Complete details of digital multiplexer No. 1 are given in Figure 11 and component location details are given in Figure 12. Type SN54153 dual four-line to one-line multiplexers are used (eight required per board). Since digital multiplexer No. 2 is identical to No. 1, one drawing is adequate for both. For three out of each four inputs line terminating components are used. These consist of a series 100 ohm resistor, a shunt capacitor of 220 picofarad and a resistor of 47 kilohm to the supply line (guarantees "1" state when input line is open circuit). Line terminations are used mainly to meet the requirements of digital multiplexer No. 2 which multiplexes three 16-line inputs from external equipment.

The type SN54153 incorporates two multiplexing units which effectively transfer the logic level at one of four inputs to the output in each case. Control inputs X_0 and X_1 (Fig. 11) gate the multiplexer inputs as indicated in the table on page 12. These control inputs are generated in the programmer described in Section 6.2.

Information Relevant to Digital Multiplexer No. 1

	MUX 1 Output Notation		a_0	a_1	a_2	a_3	a_4	a_5	a_6	a_7	a_8	a_9	a_{10}	a_{11}	a_{12}	a_{13}	a_{14}	a_{15}
Frame 0	Relevant MUX 1 input	Description	2-bit identifier		Time-of-day: Minutes							Seconds						
		Notation	a_{0_0}	a_{1_0}	a_{2_0}	a_{3_0}	a_{4_0}	a_{5_0}	a_{6_0}	a_{7_0}	a_{8_0}	a_{9_0}	a_{10_0}	a_{11_0}	a_{12_0}	a_{13_0}	a_{14_0}	a_{15_0}
		Value	0	0	×	×	×	×	×	×	×	×	×	×	×	×	×	×
Frame 1	Relevant MUX 1 input	Description	2-bit identifier		Time-of-day: Hours						Fixed data: Day-of-month							
		Notation	a_{0_1}	a_{1_1}	a_{2_1}	a_{3_1}	a_{4_1}	a_{5_1}	a_{6_1}	a_{7_1}	a_{8_1}	a_{9_1}	a_{10_1}	a_{11_1}	a_{12_1}	a_{13_1}	a_{14_1}	a_{15_1}
		Value	0	1	×	×	×	×	×	×	×	×	×	×	×	×	—	—
Frame 2	Relevant MUX 1 input	Description	2-bit identifier		Month-of-year						Fixed data: Run number (first two digits)							
		Notation	a_{0_2}	a_{1_2}	a_{2_2}	a_{3_2}	a_{4_2}	a_{5_2}	a_{6_2}	a_{7_2}	a_{8_2}	a_{9_2}	a_{10_2}	a_{11_2}	a_{12_2}	a_{13_2}	a_{14_2}	a_{15_2}
		Value	1	0	×	×	×	×	×	—	×	×	×	×	×	×	×	×
Frame 3	Relevant MUX 1 input	Description	2-bit identifier								Fixed data: Run number (last two digits)							
		Notation	a_{0_3}	a_{1_3}	a_{2_3}	a_{3_3}	a_{4_3}	a_{5_3}	a_{6_3}	a_{7_3}	a_{8_3}	a_{9_3}	a_{10_3}	a_{11_3}	a_{12_3}	a_{13_3}	a_{14_3}	a_{15_3}
		Value	1	1	—	—	—	—	—	—	×	×	×	×	×	×	×	×

"×" means information bit (may be "0" or "1").

"—" means spare bit (at present the corresponding inputs are left open circuit and are thus encoded as ones).

Control inputs		Data inputs transferred to outputs a_0 to a_{15}
X_1	X_0	
0	0	$a_{0\ 0}$ to $a_{15\ 0}$
0	1	$a_{0\ 1}$ to $a_{15\ 1}$
1	0	$a_{0\ 2}$ to $a_{15\ 2}$
1	1	$a_{0\ 3}$ to $a_{15\ 3}$

Digital multiplexer No. 2 accepts the following 16-line inputs (Fig. 11):

(i) $b_{0\ 0}$ to $b_{15\ 0}$ derived from the output of the analogue to digital converter (ADC) via front panel connector J608;

(ii) $b_{0\ 1}$ to $b_{15\ 1}$ internally connected within the data processor to the outputs a_0 to a_{15} of digital multiplexer No. 1;

(iii) $b_{0\ 2}$ to $b_{15\ 2}$ coupled to external digital transducer No. 1 (or any other external device with parallel digital output) via front panel connector J604;

(iv) $b_{0\ 3}$ to $b_{15\ 3}$ coupled to external digital transducer No. 2 (or any other external device with parallel digital output) via front panel connector J605.

Inputs $b_{0\ 0}$ to $b_{15\ 0}$ which are associated with the ADC comprise a four-bit multiplier or range indicator ($b_{0\ 0}$ to $b_{3\ 0}$ where $b_{0\ 0}$ is the most significant bit) and a 12-bit magnitude expressed in offset binary format ($b_{4\ 0}$ to $b_{15\ 0}$ where $b_{4\ 0}$ is the most significant bit). The two most significant range bits are taken to the programmer (Section 6.2) and their digital value is modified if an over-range is indicated by the ADC. Range indicator inputs $b_{0\ 0}$ and $b_{1\ 0}$ are therefore derived from the programmer output. Inputs $b_{2\ 0}$ to $b_{15\ 0}$ are taken directly from the ADC output.

Digital transducer inputs $b_{0\ 2}$ to $b_{15\ 2}$ and $b_{0\ 3}$ to $b_{15\ 3}$ may be connected as desired to the transducer sources. Input resistors connected to the supply line on the digital multiplexer board guarantees a "1" state for inputs which are open circuit. Any high frequency noise present on the input lines from the digital transducers (and also from the ADC) tends to be filtered out by the series resistance and shunt capacitance line terminations on the multiplexer board.

Control inputs Y_0 and Y_1 (Fig. 11) switch multiplexer No. 2 as indicated in the following table. These control inputs are generated in the programmer described in Section 6.2.

Control inputs		Data inputs transferred to outputs b_0 to b_{15}
Y_1	Y_0	
0	0	$b_{0\ 0}$ to $b_{15\ 0}$
0	1	$b_{0\ 1}$ to $b_{15\ 1}$
1	0	$b_{0\ 2}$ to $b_{15\ 2}$
1	1	$b_{0\ 3}$ to $b_{15\ 3}$

As will be indicated in Section 6.2 the time for which digital multiplexer No. 2 is switched to the ADC output is set to allow a preset number of words to be recorded per frame from this source whereas only one word may be recorded per frame from each of the digital transducers and from the time-of-day and fixed data digital multiplexer No. 1.

Outputs b_0 to b_{15} of digital multiplexer No. 2 are taken directly to the parallel to serial converter (Section 6.3).

6.2 Programmer

In this section the functions performed by printed circuit board 6 are described. Some functions, also of a "programming" nature are performed by the parallel to serial converter (printed circuit board 7) but these are described in detail in Section 6.3.

The block schema of Figure 10 indicates in broad detail the functions performed by the programmer and also the relationships of the programmer to the digital multiplexers and the parallel to serial converter. These functions include:

(i) using the outputs from front panel thumbwheel switches S8A and S8B to preset the number of analogue channels multiplexed (by the Dynamics Systems Electronics Model 480001 airborne multiplexer/ADC– Figure 1);

(ii) using the output from front panel switch S8C to preset the number of separate 16-line digital inputs which are time multiplexed;

(iii) provision of a five-line address output for use with the analogue multiplexer mentioned in (i) above;

(iv) provision of control signals (X_0, X_1, Y_0 and Y_1) for use with digital multiplexers Nos 1 and 2;

(v) provision of a frame synchronizing signal for use with the parallel to serial converter;

(vi) synchronization of the programmer with time-of-day signals from the time code generator;

(vii) generation of a four-line range input for the ADC when it is operated in the "programmed range" mode;

(viii) processing of an over-range flag bit (generated by the ADC) in a manner which allows recognition of the over-range condition from the recorded four-bit range.

Square wave signals derived from the master clock signal generator (Section 3.2) are taken to the "Word Rate" thumbwheel switch S11 on the data processor front panel. Digital recording rates are preset by this switch. For serial type digital recording a word (which includes 16 information bits) is recorded for every 20 cycles of the selected clock signal and for parallel digital recording a word is recorded for every four cycles. Details of the clock frequencies provided and the word rates obtainable at the various tape speeds are given in the following table.

S11 switch position	Selected clock frequency (Hz)	Word rate for serial system (word/sec)	Word rate for parallel system (word/sec)	Minimum tape speed (inch/sec)
6	40960	2048	10240*	
5	20480	1024	5120*	60
4	10240	512	2560*	30
3	5120	256	1280	15
2	2560	128	640	$7\frac{1}{2}$
1	1280	64	320	$3\frac{3}{4}$
0	640	32	160	$1\frac{7}{8}$

* These rates exceed the capability of the ADC manufactured by Dynamics Systems Electronics.

In Figure 13 full circuit details of the programmer are provided and component location details are given in Figure 14.

Division of the selected clock frequency to obtain a word rate clock signal (designated U4 in Figure 13) is performed by the bit counter (Fig. 10) in the serial system and by the byte counter in the parallel system. The first part of this counter (divide-by-ten for the serial system and divide-by-two for the parallel system) is included in the parallel to serial converter and the second part Q606A (divide-by-two) is included in the programmer.

Alternate gating of the word rate clock to the digital word counter (comprising flip-flops

Q612A and Q612B) and then to the analogue word counter (comprising decade counters Q604 and Q608, and four-bit binary counter Q613) is achieved using flip-flop Q606B. Front panel thumbwheel switches S8A and S8B enable the number of clock pulses counted during each gate period by the analogue and digital word counters respectively to be preset. One complete frame of data is generated during each gate period.

Define the successive word periods associated with each frame period as W_r where r is a subscript which is "0" for the first period and has a maximum value dependent on the numbers preset by thumbwheel switches S8A and S8B. In a logical context W_r is a quantity which is high during the period associated with the rth word and low at other times.

At the end of each frame period the Q outputs of the digital counter comprising Q612A and Q612B are both set to the low state and the Q output of gating flip-flop Q606B switches from the low state to the high state. When the Q output of Q606B is high the J input of Q612A is high (K input permanently high) and the next clock pulse U4 delivered to the clock (T) input of Q612A will cause this flip-flop to toggle.

The digital word counter will continue counting input clock pulses until gating flip-flop Q606B changes state. Decoding of the outputs of this counter is accomplished with the four NAND gates comprising Q614. The outputs (S8C-0 to S8C-3) of these gates are normally high but switch to the low state at count states 1, 2, 3 and 0 respectively. Thumbwheel switch S8C is a single pole switch with positions 0, 1, 2 and 3 only used. The wiper of this switch is returned to NAND gate Q603D via input line designated S8C-W (Fig. 13). A transition to the low state on this line causes gating flip-flop Q606B to change state and the digital word counter to be reset to the 0 state. NAND gate Q603D, capacitor C608, resistor R615 and inverter Q607F form a pulse stretching arrangement which generates an output pulse of about 170 ns duration. Capacitor C609 prevents a reset pulse being initiated by very short duration input pulses which may be generated at other than the required times because of delays between the switching of the two flip-flops comprising the digital word counter. The output of inverter Q607F switches to the low state for the duration of the reset pulse and resets the gating flip-flop Q606B (Q output switches to the low state). Similarly the output of NOR gate Q602B switches low for the duration of the reset pulse and sets the digital word counter to the 0 state. In addition Q602B generates a reset pulse when the output of inverter Q601A switches to the high state at times to be specified later.

When the gating flip-flop Q606B changes state at the time of arrival of the reset pulse indicated above, word rate clock pulses are delivered to decade counter Q604 which forms part of the analogue word counter. At the time of arrival of the reset pulse the first input clock pulse is propagated to the decade counters (Q604 and Q608) causing them to switch from count state 99 to count state 00. Subsequent input clock pulses cause the count state to advance.

The decade counters generate a 1–2–4–8 binary coded decimal output which is decoded using Q605 and Q611. As each decade counter switches through states 0 to 9 the output on lines S8B-0 to S8B-9 (units) and S8A-0 to S8A-9 (tens) switch successively from a normally high state to the low state (for one word duration except at the time of resetting the decade counters). Output lines from the BCD to decimal decoders Q605 and Q611 are taken respectively to switches S8A and S8B (10 position single-pole type) and the wipers of these are returned to inputs of NOR gate Q602A. When the decade counters reach the count state preset on S8A and S8B thumbwheels, a transition to the high state occurs at the output of Q602A. At the time of this transition gating flip-flop S606B changes state, decade counters Q604 and Q608 are reset to count state 99 and the four-bit binary counter Q613 is reset to count state 00. NAND gate Q603A, capacitor C603, resistor R603 and NOR gate Q602C form a reset pulse stretching arrangement which generates an output pulse of about 540 ns duration. (Normally the output of inverter Q601B is low.) Capacitor C604 prevents a reset pulse being initiated by very short duration input pulses which may be generated at other than the required times because of propagation delays through the decade counters.

Selection of any analogue input channel connected to the analogue multiplexer/ADC equipment (Figs. 1 and 10) may be made via a five-line address (random mode of operation). This equipment has 32 analogue channels. The required address outputs are binary equivalents of 0 through 31. To generate these address outputs m_0 to m_4 (Fig. 13), the four-bit binary counter Q613 is clocked by the "A" output of decade counter Q604. The frequency of this output is half that of the input clock to Q604. Inverters are used to buffer the address outputs.

The analogue word counter reset pulse is also taken via NOR gate Q602B to the digital word counter reset inputs. Normally the digital word counter is in the reset ("0") state at the time of arrival of this pulse. However, it ensures that no change of state occurs in the digital word counter until one word period has elapsed since the reset pulse was generated.

In the following table the address outputs, the digital word counter outputs and the gate output are given as a function of word period where N_D = number preset on digital channels selector switch S8C ($0 \leqslant N_D \leqslant 3$), N_A = number preset on analogue channels selector switches S8A and S8B ($0 \leqslant N_A \leqslant 32$ for serial system and $0 \leqslant N_A \leqslant 31$ for parallel system).

Details relevant to the data which are serialized during each word period are also given in the table. The table has been drawn up to $N_D = 3$. For $N_D = 2$ omit W_3; for $N_D = 1$ omit W_2 and W_3; for $N_D = 0$ omit W_1, W_2 and W_3.

Word period	Gate* output	Digital word counter outputs		Address outputs from analogue word counter					Operations performed
		Y_1	Y_0	m_4	m_3	m_2	m_1	m_0	
W_0	1	0	0	0	0	0	0	0	Sync. word. No encoding of data for serial system. Encode data for analogue channel address N_A for parallel system.
W_1	1	0	1	0	0	0	0	0	Encode data from digital multiplexer 1 (used for time-of-day and fixed data).
W_2	1	1	0	0	0	0	0	0	Encode data for digital transducer No. 1.
W_3	1	1	1	0	0	0	0	0	Encode data for digital transducer No. 2.
W_4	0	0	0	0	0	0	0	1	Encode data for analogue address 0.
W_5	0	0	0	0	0	0	1	0	Encode data for analogue address 1.
↕									
$W_{N_D+N_A-1}$	0	0	0	$N_A - 1$					Encode data for analogue address ($N_A - 2$).
$W_{N_D+N_A}$	0	0	0	N_A					Encode data for analogue address ($N_A - 1$).
W_0	1	0	0	0	0	0	0	0	Sync. words (details given above).

* Q output of Q606B.

From the above table it is apparent that N_D equals the number of digital channels (apart from the ADC output) encoded in each frame. Similarly N_A equals the number of analogue

channels encoded in each frame for the serial system and $N_A + 1$ is the corresponding number for the parallel system.

The number of words recorded per frame (including the synchronizing word W_0) is equal to $N_D + N_A + 1$. For $N_D = 0$ the ADC output only is recorded. For $N_A = 0$ no recording of data from the ADC takes place for the serial system and the data for only one channel (address 0) are recorded for the parallel system.

At the beginning of each frame period the logic states (as indicated in the above table) corresponding to W_0 are always generated regardless of the values of N_D and N_A. NOR gate Q602D generates an output pulse W_0 which is high for the duration of the first word period in the frame. W_0 is inverted using Q609F to give $\overline{W_0}$ which is used as a frame synchronizing pulse (Section 6.3).

W_0 is also taken to the clock input of flip-flop Q615B forming the first stage of the frame counter (which divides the frame rate input clock frequency by four). Capacitor C610 prevents the frame counter from responding to very short duration input pulses which may be generated because of propagation delays associated with the switching of gating flip flop Q606B, the digital word counter Q612 and associated decoder. Control outputs X_0 and X_1 from the frame counter are used in conjunction with digital multiplexer No. 1 (used for multiplexing time-of-day and fixed data).

Both the time code generator and the digital circuits discussed in these sections derive their basic timing from the master clock signal generator. Time-of-day, which is recorded once every four frames of data, provides one second resolution. Because an integral number of words are always recorded per second, interpolation may be used to enable better time resolution to be obtained when the data are read at the ground station. Furthermore, FM data (Section 4.2) are also multiplexed at rates defined by the master clock signal generator. To demultiplex such data at the ground station the recorded time signals are used. It is imperative that the actual word time, during which the "second" advance occurs in the time code generator, be recognizable, particularly when the FM data are multiplexed at the higher rates available. To make this recognition possible it is essential that the digital circuits under discussion in this section be synchronized to the time code generator output.

Input time synchronizing signals TS1, TS2 and TS3 corresponding respectively to outputs from the time code generator with 1, 2 and 10 second repetition period are taken to the programmer. When the time registered by the time code generator advances in 1, 2 and 10 second steps respectively a transition to the high state will occur on the corresponding synchronizing input. Selection of any one of the time synchronizing inputs is via a link (Fig. 13).

For correct synchronization to be achieved with the ground station reduction equipment the programmer must switch to the logical states indicated in the previous table for W_1, at the time a positive transition occurs on the selected time synchronization input. To achieve this, digital word counter Q612A is preset and all others (including the portion of the bit counter in the parallel to serial converter) are cleared. The preset pulse is derived from the output of inverter Q607E and the clear pulses are derived from the output of inverter Q601C. The duration of the preset pulse coupled to Q612A is made longer than the clear pulse to that counter and hence the preset pulse takes control.

Usually the number of words per frame is chosen such that an integral number of four-frame periods occur per period of the time synchronizing signal. In that case time synchronizing pulses received subsequent to the first one during a recording run will serve only to check that the circuits are correctly set. The following table indicates the number of time readings (i.e. number of four-frame durations) which occur per time synchronizing period at the lowest recording rates available (32 words per second for the serial system).

To prevent incorrect resetting of the digital word counter by the time synchronizing pulse when $N_D = 3$ it is essential that the pulse duration defined by C603 and R603 be of sufficient duration to be maintained while the decoded "0" state pulse from this counter is propagated via C608 and R615. If this condition is not satisfied the decoded "0" state pulse will cause gating flip-flop Q606B to switch to the analogue word counter rather than the digital word counter (i.e. to W_1 rather than W_0).

Range determination for the ADC may be either automatic or programmed. Data processor front panel switch S9 enables the method of range determination to be selected. The logic level on a control line (1 for automatic and 0 for programmed) performs the appropriate selection.

Words per frame (incl. sync. word W_0)	Time readings per 1 sec	Time readings per 2 sec	Time readings per 10 sec
1	8	16	80
4	2	4	20
5	1·6	3·2	16
8	1	2	10
10	0·8	1·6	8
16	0·5	1	5
20	0·4	0·8	4

When programmed range determination is employed a four-line address is taken from the data processor to the ADC. Eleven ranges as indicated in the following table may be selected.

Thumbwheel switch position	Range (V)	Range select signal			
		PR4	PR3	PR2	PR1
0	10·24	0	0	0	0
1	5·12	0	0	0	1
2	2·56	0	0	1	0
3	1·28	0	0	1	1
4	0·64	0	1	0	0
5	0·32	0	1	0	1
6	0·16	0	1	1	0
7	0·08	0	1	1	1
8	0·04	1	0	0	0
9	0·02	1	0	0	1
10	0·01	1	0	1	0

Although a separate range may be programmed for each analogue input, the data processor allows only one to be selected for all inputs. A single-pole 11-position thumbwheel switch S10 is used for programmed range selection. Switch outputs 1 to 10 are taken to programmer inputs S10-1 to S10-10 and the switch wiper is connected to digital common ("0" level). Coding of the programmed range inputs to the ADC (designated as PR1, PR2, PR3 and PR4 in the above table and also in Figure 13) is performed using quad input NAND gates Q617A, Q617B, Q618A and Q618B, inverters Q607D and Q609A, and dual input NAND gates Q616C and Q616D. Resistors R616 to R625 guarantee that open circuit inputs will be read as ones.

The four-bit range indicator, which is internally generated in the ADC when automatic ranging is used or which is received from the data processor when programmed ranging is used, forms the four most significant bits of the 16-bit output from the ADC. In order of significance, these bits are defined as b_{0A}, b_{1A} (Fig. 13), b_{2-0} and b_{3-0} (Fig. 11). b_{0A} to b_{3-0} may take on the digital values defined for PR4 to PR1 respectively in the above table.

The ADC generates an over-range flag bit (in addition to the 16-bit output providing range, sign and magnitude information) which indicates whether the signal has exceeded the range maximum at the time the conversion is completed. A high level on the flag line indicates an over-range condition has occurred. The over-range indication is meaningful only when programmed ranging is used.

To provide a recorded indication of the over-range condition the two most significant range bits are both set high if an over-range occurs. Both these bits are never high simultaneously in the four-bit range received from the ADC as may be observed in the above table. When the

recorded data are reproduced at the ground station these range bits are first examined by the computer and if both are set the particular reading is ignored.

The over-range flag input (O/R—Fig. 13) and the complements ($\overline{b_{0A}}$ and $\overline{b_{1A}}$) of the two most significant range inputs are processed using NAND gates Q603C, Q616A and Q616B to provide the two most significant range inputs b_{0_0} and b_{1_0} for digital multiplexer No. 2 (Fig. 11). If processing of the over-range bit is not required a link at the input of Q603C as indicated in Figure 13 may be connected to digital common.

The O/R CONTROL input (Fig. 13) causes the over-range flag input O/R to be ignored when the ADC is operated with automatic range. Front panel mounted toggle switch S9 sets the level on the O/R CONTROL low for automatic range and high for programmed range operation. A link at the input of Q603C connects the O/R CONTROL to the over-range processing circuit. Hence outputs b_{0_0} and b_{1_0} will differ from inputs b_{0A} and b_{1A} only if the over-range flag bit is high and programmed ranging is employed.

6.3 Parallel to Serial Converter

6.3.1 General Considerations

A hybrid recording system,[1] for which both analogue and digital type recording are performed using the same analogue tape machine, has been adopted. At present a seven-track tape machine (an Ampex Model AR200), designed for use in airborne applications, has been fitted with recording amplifiers suitable for serial type recording. Either one or two tracks are allocated for serial type recording. Non-return-to-zero-mark (NRZM) recording and return-to-zero (RZ) recording have been made available as alternatives.[8] When NRZM recording is used two recording tracks, one for the data and one for odd lateral parity, are used since the basic code is not self-clocking. When RZ recording is used only one recording track is used as this code is self-clocking.

The serial digital output from the data processor could be recorded using other transports with the same or a different number of tracks (even a single track cassette type) if suitable recording amplifiers were provided.

Because only one tape track is required RZ type recording is normally used in preference to NRZ recording. RZ format has been chosen in preference to other self-clocking formats (e.g. phase encoding) because recorded "ones" and "zeros" yield signals having the same frequency component. This property proves advantageous when the data are to be reproduced over a wide range of tape speeds using flywheel techniques to detect synchronizing gaps.[13]

When digital recording only is required and when higher rates than those obtainable for serial type recording at equivalent tape speed, are necessary, parallel type digital recording may be employed. However, fitting of an in-line recording head (in lieu of the standard staggered headstack) would be necessary for parallel recording using the Ampex AR200 transport. Alternatively a different transport with a standard in-line head fitting could be used. Circuit hardware which will allow parallel recording (using a seven-track transport) of digital data has been incorporated in the data processor.

Since the digital information to be recorded is in the form of 16-bit parallel words it is essential that parallel to serial conversion be performed for both serial and parallel forms of recording. For serial recording 16 serial information bits are generated per word and four serial bytes are generated for parallel recording. To accommodate the different requirements of the two recording systems separate printed circuit boards (designated 7A and 7B) are used.

The block schema of Figure 10 indicates in broad detail the functions performed by the parallel to serial converter (for either serial or parallel systems) and also the relationship of the parallel to serial converter to the programmer and the digital multiplexers. These functions include:

(i) counting of input clock pulses from the master clock signal generator by the bit/byte counter;
(ii) decoding of the bit/byte counter outputs to provide control signals for the serializer and the output format generator;
(iii) generation of a "command to convert" output for use with ADC;
(iv) Serialization of the digital data (which are received as 16-bit parallel words);

(v) generation of parity checkbits as required;
(vi) generation of appropriate output format which includes frame synchronizing information.

The two circuits, for the serial and the parallel systems respectively, will now be considered separately.

6.3.2 Serial System

Full circuit details of the parallel to serial converter for the serial system are given in Figure 15 and component location details are given in Figure 16.

A square wave input clock signal C_L (Fig. 15) is derived from the "word rate" front panel switch S11 which selects one of seven signals taken from the master clock signal generator. Details of the clock frequencies available (640 Hz to 40·960 kHz) and the word rates obtainable at the various tape speeds have been tabulated in Section 6.2. For serial type recording a word is recorded for every 20 cycles of the input clock. Division of the input clock frequency by 20 to obtain a word rate clock is performed by the bit counter comprising decade counter Q701 (contained in the parallel to serial converter—Figure 15) and divide-by-two flip-flop Q606A (contained in the programmer—Figure 13).

Define the successive "bit" periods associated with each word period as B_r where r is a subscript which is "0" for the first period and "19" for the last period. In a logical context B_r is a quantity which has a value "1" for the time associated with bit period B_r and a value "0" at other times. For convenience in describing bit counter decoding logic define the digital outputs (Fig. 15) of the bit counter as a, b, c, d and e. (Note that d = U3 and e = U4 [Fig. 15].) In the following table the logical values of the digital outputs together with the operations performed are given as a function of bit period.

Serialization of the digital data (one bit at a time) is accomplished using the 16-bit shift register comprising Q708 and Q709. The 16-line output from digital multiplexer No. 2 (b_0 to b_{15}) is loaded in parallel into the shift register as indicated in Fig. 15 and "right" shifted one bit at a time to the Q output of Q709. Each time the shift register receives a clock pulse, while the clock inhibit lines are low, a right shift of one place occurs.

As indicated in the above table 18 bits are encoded for each word; b_0 to b_{15} correspond to the digital inputs to the parallel to serial converter, b_{16} is a "dummy" bit which is always "0" and b_{17} is an even longitudinal parity checkbit. At the beginning of each word period a two-bit duration gap (no digital information encoded) is inserted to allow for word synchronization.

The parallel to serial converter of Figure 15 provides alternative NRZM (two-line) or RZ (one-line) outputs. The two NRZM outputs comprise a data signal and an odd lateral parity signal (which may also be referred to as a non-return-to-zero-space [NRZS] signal as per IRIG[4]). Use of the odd parity output ensures that a change of state occurs on one of the two NRZ lines for each bit recorded. Hence clock pulses may be generated by ground station data reduction equipment to allow the recorded NRZ data to be read. By encoding the extra dummy bit b_{16}, even longitudinal parity checkbits may be encoded on both NRZ outputs and at the same time satisfy the odd lateral parity requirement.

Input clock signal C_L is inverted by Q704F to give $\overline{C_L}$ (where the "bar" is the inverting notation) which is used to clock decade counter Q707 (the first part of the bit counter). Switching of Q701 is in synchronism with the positive transitions of $\overline{C_L}$ (where "positive" refers to the slope). Hence the bit, word and frame counters will switch in synchronism with the positive transitors of $\overline{C_L}$ (with due allowance for propagation delays inherent in these "ripple through" counters).

$\overline{C_L}$ is taken to the input A_1 of monostable multivibrator Q711 (also referred to as "single shot") which generates negative going (meaning a change from high to low) pulses of about 1 μs duration. At the trailing edges of these pulses (i.e. about 1 μs after $\overline{C_L}$ switches high) negative going pulses of about 260 ns duration are initiated at the output of inverter Q704A. These latter pulses are taken to the clock inputs of the shift register comprising Q708 and Q709. Right shifting of the data stored in the register takes place in synchronism with the positive edge of the register input clock or effectively at the trailing edge of the pulse generated at the output of inverter Q704A.

Bit period	Bit counter logical outputs					Operations performed		
	e	d	c	b	a			
B_{19}	0	0	0	0	1	End of Word Period, Encode Longitudinal Parity Bit b_{17}	*2 *3	
B_0	0	0	0	0	0	Start of New Word, Load Data from Dig Mux 2 into Shift Register	*1	
B_1	0	0	0	0	1	Start Conversion in ADC		
B_2	0	0	0	1	0	Encode b_0		Data bits
B_3	0	0	0	1	1	Encode b_1		
B_4	0	0	1	0	0	Encode b_2		
B_5	0	0	1	0	1	Encode b_3		
B_6	0	0	1	1	0	Encode b_4		
B_7	0	0	1	1	1	Encode b_5		
B_8	0	1	0	0	0	Encode b_6		
B_9	0	1	0	0	1	Encode b_7		
B_{10}	1	0	0	0	0	Encode b_8		
B_{11}	1	0	0	0	1	Encode b_9		
B_{12}	1	0	0	1	0	Encode b_{10}		
B_{13}	1	0	0	1	1	Encode b_{11}		
B_{14}	1	0	1	0	0	Encode b_{12}		
B_{15}	1	0	1	0	1	Encode b_{13}		
B_{16}	1	0	1	1	0	Encode b_{14}		
B_{17}	1	0	1	1	1	Encode b_{15}		
B_{18}	1	1	0	0	0	Encode b_{16} (b_{16} = 0, dummy bit)		
B_{19}	1	1	0	0	1	Encode b_{17} (b_{17} = long. parity bit)		

*1—Insert interword gap (no data encoded).
*2—Inhibit output clock.
*3—Inhibit shift register clock.

Note: b_0 to b_{15} as included in this table represent the digital values loaded in parallel into the shift register.

Monostable multivibrator Q711 delays the shifting of data in the register till after the bit counter has had time to settle to a new state. Decoding of the bit counter is used to generate the

clock inhibit signal for the shift register. Hence any ambiguity in the number of uninhibited clock pulses received per word is removed with the time delay.

Decoding of the bit counter outputs is necessary to establish the sequence of operations listed in the previous table.

The first requirement is to load the 16-line output b_0 to b_{15} from digital multiplexer No. 2 into the shift register (referred to as "serializer" in Figure 10). To allow the data outputs from the multiplexer to settle after a new 16-line input has been selected (multiplexer switching takes place at the leading edge of B_0), it has been found convenient to delay the load pulse half a bit period after the leading edge of B_0. As depicted in Figure 17 a load pulse of about 280 ns duration is generated at the output of inverter Q704D. Transfer of data to the shift register takes place on the negative edge of the load pulse (i.e. when the output of Q704C, having logical value B_0C_L, goes high). Reference to the circuit diagram of Figure 15, on which the important logical outputs are marked symbolically, and also to the previous table, will enable the decoding sequence to be readily followed.

A command-to-convert signal CTC (Fig. 15) for the ADC is generated at the output of inverter Q704E. Conversion is initiated by a positive transition on the CTC output line. Such a transition occurs (Fig. 17) at the end of each B_0 bit period (or alternatively at the start of each B_1 period). Filter components R701 and C701 prevent the ADC from responding to any unwanted short duration pulses generated internally in the parallel to serial converter. At the time the conversion is initiated in the ADC the address inputs m_0 to m_4 (Section 6.2) are strobed into the ADC. Since a CTC pulse is generated for every word (including those associated with frame synchronization [W_0], time-of-day and fixed data [W_1], and digital transducer output data [W_2 and W_3]) a conversion will be performed in the ADC for every word. Encoding of the data generated by the ADC takes place during the word period following that during which the conversion takes place.

During bit periods B_{19}, B_0, B_1 and B_2 it is necessary to inhibit the shift register clock (Fig. 17). A high state on the clock inhibit lines to the shift register prevents shifting of the data when clock pulses are received. As indicated in Figure 15 the required inhibit signal $B_{19} + B_0 + B_1 + B_2$ is generated at the output of NAND gate Q706D.

During bit periods B_{19}, B_0 and B_1 it is necessary to prevent the transfer of output clock pulses (as generated at the Q output of Q710—Figure 17) to either of the output flip-flops (Q712A or Q712B) used for generating the NRZ output signals. Except during the frame synchronizing period W_0 the output of NAND gate Q707D is high and the output of NAND gate Q703A is $B_{19} + B_0 + B_1$. This latter output (Fig. 17) prevents the generation of positive going output clock pulses (5 μs duration chosen in view of the needs of the RZ recording system) at the output of NOR gate Q705B. Details of the serialized outputs coded in NRZ format are given in Figure 18. Output NRZ1 ("data" output) changes state when ones are encoded and output NRZ2 ("odd parity" output) changes state when zeros are encoded. During bit period B_2, information bit b_0 is encoded and so on up to b_{17} during consecutive bit periods. Since the "serial input" of shift register Q708 is connected permanently to the low state, the "dummy" bit b_{16} is always encoded as a "0". During bit period B_{19} even longitudinal parity bits are encoded on both the NRZ1 and the NRZ2 outputs. If an odd number of ones has been encoded during bit periods B_2 to B_{18} then a one is encoded during bit period B_{19}. Both NRZ outputs switch in synchronism with the trailing edges of the output clock pulses.

To encode the longitudinal parity bit, the trailing edge of the 5 μs pulse generated at the output of NOR gate Q705D during B_{19}, initiates a pulse (Fig. 17) of about 280 ns duration (at the output of inverter Q713C) for resetting the output flip-flops to the "0" state. No change of state takes place in the output flip-flop (Q712A or Q712B) which is in the "0" state at the arrival of the reset pulse.

Inverters Q704B and Q704C buffer the outputs NRZ1 and NRZ2 which are taken to the NRZ digital recording amplifiers[8] associated with the analogue tape recorder. Hence just after the longitudinal checkbit is encoded both the NRZ1 and the NRZ2 outputs will be high.

An RZ output is generated at the same time as the NRZ outputs are generated. Whenever a one is encoded a negative going pulse of 5 μs duration is generated at the output of inverter Q713D. Similarly whenever a zero is encoded a negative going pulse is generated at the output of inverter Q713C.

A discrete component switching circuit comprising transistors Q715 to Q718 and associated

components accepts the outputs of inverters Q713D and Q713A and generates an RZ output as illustrated in Figure 18. The form of the RZ output is similar to that mentioned by Weber[11] but differs from that mentioned by IRIG.[4] Whenever a one is encoded a positive pulse (switching between the limits of 0 V and 5 V approximately) is generated at the RZ output and whenever a zero is encoded a negative pulse (switching between the limits of 0 V and −5 V) is generated at the RZ output. In each case pulses generated at the RZ output are in time synchronism with the output clock (Q output of Q710) pulses. The RZ output pulses have a duration of about 5 μs which remains unchanged regardless of the data rate which is employed. The RZ output of the parallel to serial converter is taken to the RZ digital recording amplifier[8] associated with the analogue tape machine.

Insertion of suitable synchronizing information into the digital output signals from the parallel to serial converter is necessary to enable reading of the data at the ground station. As indicated in Figure 18 no information is encoded during bit times B_0 and B_1. Hence an inter-word "gap" equivalent to two-bit durations indicates that a new word is about to be encoded. Such a gap is recognized by the ground station equipment and is used to synchronize the serial to parallel converter used in that equipment.

Similarly, suitable frame synchronizing information must be encoded to allow identification of individual words by the ground station equipment. As indicated earlier word period W_0 is used for encoding frame synchronizing information. Two alternative systems (which will be referred to as system A and system B respectively) have been provided. Removal of or insertion of a link situated at the input of Q707D (Fig. 15) allows selection of system A or system B respectively.

When system A is used the output of NAND gate Q707D is W_0 and that of NAND gate Q703A is $W_0 + B_0 + B_1 + B_{19}$ as illustrated in Figure 19. Hence for the complete duration of W_0 no output data are encoded. This system of frame synchronization has been adopted in the serial data generator described elsewhere.[12] Checking of the ground station digital interface equipment[13] is performed with the aid of the serial data generator.

In system B (Fig. 20) the output of NAND gate Q703A becomes $W_0a + B_0 + B_1 + B_{19}$. Hence for the duration of W_0 the output clock is inhibited when "a" (A output of decade counter Q701) is high. One of the main advantages of this system of frame synchronization is that a regular clock every four-bit durations (as indicated by dotted lines in Figure 20) corresponding to B_2, B_6, B_{10}, B_{14} and B_{18} is generated continuously. Provision of this regular clock is a requirement for demultiplexing FM data (particularly when high sampling rates are employed) using ground station equipment.

Early tests with the Dynamics Systems Electronics equipment indicated that it was possible for that equipment to lock-out (not respond to any external control inputs) at power switch-on. A transition from low to high on its RESET input will initiate operations if that condition exists. Spare gates Q109B and Q113B on the analogue multiplexer control signal generator (Fig. 4) have been used to generate suitable reset signals for serial and parallel systems respectively. Selection of the appropriate reset signal (SER-RESET or PAR-RESET) is made via links on the parallel to serial converter boards (Figs. 15 and 21).

6.3.3 Parallel System

Full circuit details of the parallel to serial converter for the parallel system are given in Figure 21 and component location details are given in Figure 22.

The square wave input clock signal C_I (Fig. 21), identical to that used for the serial system, is inverted by Q763A and the output C_I is taken to the byte counter which divides the frequency by four. Flip-flops Q760B (Fig. 21) and Q606A (Fig. 13), which are each connected as divide-by-two circuits, constitute the byte counter. A word is encoded for every four cycles of the input clock.

Define the successive "byte" periods associated with each word period as B_r where r is a subscript which is "0" for the first byte period (in the word period) and "3" for the last period. In a logical context B_r has the same meaning as defined in Section 6.3.2 for the bit periods.

As indicated in Figures 21 and 13 the byte counter outputs are represented by U3 and U4. In the following table the logical values represented by the digital outputs together with the operations performed are given as a function of byte period.

Byte period	Byte counter logical outputs		Operations performed
	U4	U3	
B_0	0	0	Encode b_0, b_1, b_2 and b_3; load data from Dig Mux. 2 into latches; start conversion in ADC.
B_1	0	1	Encode b_4, b_5, b_6 and b_7.
B_2	1	0	Encode b_8, b_9, b_{10} and b_{11}.
B_3	1	1	Encode b_{12}, b_{13}, b_{14} and b_{15}.

Seven NRZM outputs (NRZ1 to NRZ7) are generated in the parallel to serial converter. Digital information b_0 to b_{15} derived from the output of digital multiplexer No. 2 is encoded on outputs NRZ1 to NRZ4, word synchronizing information on NRZ5, frame synchronizing information on NRZ6 and odd lateral parity information on NRZ7. The arrangement used is indicated in the following table.

Output	Encoded data											
NRZ1	b_0	b_4	b_8	b_{12}	b_0	b_4	b_8	b_{12}	b_0	b_4	b_8	b_{12}
NRZ2	b_1	b_5	b_9	b_{13}	b_1	b_5	b_9	b_{13}	b_1	b_5	b_9	b_{13}
NRZ3	b_2	b_6	b_{10}	b_{14}	b_2	b_6	b_{10}	b_{14}	b_2	b_6	b_{10}	b_{14}
NRZ4	b_3	b_7	b_{11}	b_{15}	b_3	b_7	b_{11}	b_{15}	b_3	b_7	b_{11}	b_{15}
NRZ5	0	0	1	1	0	0	1	1	0	0	1	1
NRZ6	1	1	1	1	0	0	0	0	1	1	1	1
NRZ7	p	p	p	p	p	p	p	p	p	p	p	p
	Word period $\longleftarrow W_{N_D+N_A}{}^* \longrightarrow$				Word period $\longleftarrow W_0 \longrightarrow$				Word period $\longleftarrow W_1 \longrightarrow$			

* Refer to Section 6.2 for definition.
"p" signifies an odd parity checkbit (i.e. if the sum of the binary digits encoded on NRZ1 to NRZ6 is even a "1" is encoded on NRZ7).

Various control signals (Fig. 13) are generated for use with the parallel to serial converter.

At the start of byte period B_0, outputs b_0 to b_{15} from digital multiplexer No. 2 (Section 6.1) are loaded into the four-bit bistable latches Q751 to Q754. The Q outputs of the latches take on the logical states of the corresponding D inputs when the load input (applied to inputs designated "CLK") switches high. When the load input reverts to the low state the Q outputs remain at the logical states established at the time just before the load input switches low.

Decoding of the byte counter outputs to generate the logical output B_0 is performed using NOR gate Q763D. Negative going pulses of about 700 ns duration are generated at the output of buffer Q765B (connected as an inverter) in time synchronism with each positive transition of the input clock C_L. Similar pulses are generated at the output of inverter Q762C

in time synchronism with the negative transitions of the input clock C_L but only for the B_0 byte period. LOAD and CTC (command-to-convert) pulses, as indicated in Figure 23, are generated during byte period B_0. The CTC pulse initiates the conversion in the ADC at the time of the positive transition. The LOAD pulse is used for reading the digital inputs into the latches and is also taken to an output line (via series resistor R758) for possible alternative use as a CTC signal.

Digital multiplexing of the 16-line output from the latches (corresponding to bits b_0 to b_{15}) into a four-line output (designated by 1Y and 2Y in Q755 and Q756) is accomplished using Q755 and Q756. Sequential gating of the inputs four at a time, as indicated in the previous two tables, is controlled by the byte counter outputs U3 and U4.

Output flip-flops (Q757A to Q760A) encode the digital data as indicated in the previous table. All outputs are in NRZM format.

Clock signals (Fig. 23) for the output flip-flops are derived from buffer Q765B. Whenever the J and K inputs on any output flip-flop are both high at the time of arrival of a clock pulse that flip-flop will change state and a "1" will be encoded. Conversely no change of state will occur if the J and K inputs are both low at the time of arrival of the clock pulse and hence a "0" will be encoded. Buffering of the Q outputs of these flip-flops is provided via inverters the outputs of which are coupled via series resistors to the NRZ outputs.

Word and frame synchronizing information is encoded on outputs NRZ5 and NRZ6 respectively as indicated in the previous table. No "gaps" are employed (compare with the serial system). Byte counter output U4 is taken to flip-flop Q759A for generating the NRZ5 output. Frame synchronizing signal $\overline{W_0}$ is inverted and taken to flip-flop Q759B used for generating the NRZ6 output. Parity generator Q764 generates an odd parity bit which is encoded on the NRZ7 output using flip-flop Q760A.

Using an alternative synchronizing arrangement it would have been possible to encode a word for every three bytes. However, the marginal increase in encoding rate thus obtainable was not considered sufficient in view of the inconvenient timing which would result if the input clock were divided by three rather than four.

All of the NRZ outputs switch in synchronism with the negative transitions of the clock for the output flip-flops (Fig. 23).

Since a CTC pulse is generated for every word a conversion will be performed in the ADC during each word period. However, the ADC output may not be encoded for up to three words per frame (W_1, W_2 and W_3) depending on the setting of the "digital channels" thumbwheel. As mentioned in Section 6.2, if N_A is the number preset on the "analogue channels" thumbwheel then $N_A + 1$ words will be encoded from the ADC output for each frame. Data from analogue address N_A will be encoded during word period W_0. Hence it follows that when data are read at the ground station it is more convenient to consider data encoded during word period W_0 as being the last word in the frame rather than the first.

Longitudinal parity checkbits are not generated for the parallel system.

7. POWER SUPPLY

7.1 General Considerations

When the data acquisition equipment, which includes a number of separate units, is used in airborne applications the aircraft DC supply (+28 V nominal) provides power for each unit. The following are the main units (Fig. 1) which together constitute the data acquisition equipment:

(i) multiplexer and analogue to digital converter;
(ii) data processor (described in this report);
(iii) time display (for monitoring use only);
(iv) analogue tape recorder.

Outputs from the data processor are taken to the single-ended inputs of the analogue tape recorder. The "common" terminals of the recorder inputs are connected to chassis which in turn is connected to the "common" terminal of the supply input to the recorder. Normally the recorder is powered directly from the aircraft DC supply so that signal "commons" are grounded to the airframe via the recorder power connections (since the "common" terminal of aircraft

supplies is always grounded to the airframe). To minimize the generation of ground loop noise signals it is essential that signal "commons" in units other than the tape recorder be isolated (within each respective unit) from the aircraft supply common. To achieve this isolation separate DC to DC converters have been included in units (i) to (iii).

Since the data processor must operate from aircraft batteries (or substitute power source) when the engine-driven generators are not operating (such as may occur when the data acquisition equipment is set up prior to take-off) the unit has been designed to operate from supply inputs down to +22 V. The upper limit of the input supply voltage for satisfactory operation (constrained by the heat dissipation capability of the data processor power supply) has been made +30 V.

Considerable simplification in the power supply design for units (i) to (iii) would have resulted if the 115 V 400 Hz power available in most aircraft had been used rather than the DC power. However, since the data acquisition equipment is intended for general purpose use including also shipboard and field applications, where such AC power may not be available, a DC power source was considered preferable.

Regulated voltage supplies with current capabilities as tabulated below are available from the data processor power supply.

Regulated voltage	Maximum current capability
+5 V	4 A
+15 V	100 mA
−15 V	100 mA

The current capabilities exceed the present requirements (+5 V at about 2 A, +15 V at 65 mA, and −15 V at 50 mA) and will allow for future extensions (two unused printed circuit card spaces available at this time) if required.

The power supply (Fig. 24) for the data processor is a self-contained unit housed within the data processor unit. It may be unplugged from the data processor unit without the need for any desoldering. Two printed circuit boards, designated Part A and Part B (Fig. 24) are used. Part A is fixed relative to the power supply chassis; it contains a saturating core inverter and some components associated with the +5 V regulator. Part B plugs into the power supply unit; it contains regulating circuits for the +5 V, the +15 V and the −15 V supplies. Components in which considerable heat is generated are mounted on heatsink HS01 (Fig. 24) which is located external to the printed circuit boards. Component layout details for Parts A and B (Fig. 24) of the power supply are given respectively in Figures 25 and 26, and that for the heatsink HS01 is given in Figure 27.

7.2 DC to DC Converter

DC to DC conversion is achieved using a conventional saturating core inverter (Fig. 24) employing a common collector configuration for the switching transistors Q01 and Q02. The frequency of oscillation (at rated maximum load as tabulated in Section 7.1) is 800 Hz.

Components R01, R03 and CR01 guarantee that oscillations will commence as soon as power is applied.

To reduce the magnitude of switching transients superimposed on the square type waveform developed between the emitter of Q01 or Q02 and input common, C04 has been connected across the primary winding.

To reduce interference with other electrical equipment connected to the main aircraft or substitute supply because of switching transients, filtering with L01, C02 and C03 is used in the primary circuit. Using this arrangement the ripple fed back onto the main supply lines has been reduced.

Conventional rectifier-filter arrangements, connected to the secondary winding of the saturating core transformer L02, provide the unregulated DC inputs to the voltage regulators.

In the case of the + 5 V supply a centre-tapped winding is employed to reduce the power loss in the rectifying diodes and to allow the generation of a higher voltage for use with the + 5 V regulator Q05. Improved efficiency results from this arrangement.

Diodes CR04 and CR05 carry the main current for the + 5 V regulator and are mounted on heatsink HS01; diodes CR02 and CR03 carry only the relatively small current required for the + 5 V regulator Q05 and are mounted on board A.

7.3 Voltage Regulators

Conventional series type regulators provide the required + 5 V, + 15 V and - 15 V outputs. Integrated circuit regulating units Q05, Q07 and Q08 provide the required regulation in each case. Since these regulating units have low current carrying capacity only, the major portion of the load current, in each case, is carried by external "booster" transistors.

Two Darlington devices Q03 and Q04, connected in parallel, carry most of the load current for the + 5 V regulator, whereas transistors Q06 and Q09 carry most of the load current for the + 15 V and - 15 V regulators respectively.

Short circuit current limiting is provided for each regulated output. Preset current limits are provided according to the values of R11, R17 and R23 chosen for the + 15 V, the + 5 V and - 15 V supplies respectively. The current limits which have been provided are tabulated below.

Regulated voltage	Short circuit current
+ 5 V	5 A
+ 15 V	150 mA
- 15 V	150 mA

With the above current limits the power supply is undamaged if a sustained short circuit is applied at the output of any regulator.

Regulated + 5 V is required mainly for digital integrated circuits. Decoupling of this supply via a series inductor (27 μH) and a shunt capacitor (6·8 μF) is provided on each printed circuit board (other than those for the power supply). In each case the decoupled output of the inductor has been designated V_{CC}.

Regulated + 15 V and - 15 V are required for use with analogue signal amplifiers (used on boards 0 and 2) and for amplification of pulses (which may have either polarity at the amplifier output) in the parallel to serial converter (board 7A).

The "common" line for the + 5 V regulated output has been designated "DIGITAL COM", and that for the + 15 V and - 15 V outputs has been designated "ANALOG COM" (Fig. 24). DIGITAL COM and ANALOG COM are not connected within the power supply but are connected together on boards 0, 2 and 7A.

The measured current drawn from the + 5 V supply for each of the plug-in cards is tabulated below.

Board No.	Current from + 5 V supply
0	320 mA
1	230 mA
2	20 mA
3	400 mA
4	160 mA
5	170 mA
6	250 mA
7A	220 mA
7B	290 mA

Total current drawn from the + 5 V supply is 1·8 A approximately.

Measured currents from the + 15 V and − 15 V supplies are 65 mA and 47 mA respectively.

8. PERFORMANCE OF DATA ACQUISITION SYSTEM

The airborne data processor has been extensively tested in conjunction with the associated acquisition hardware. To assess the performance of the acquisition equipment it has also been necessary to manufacture and test associated data reduction hardware.

Extraction of speech and a tape speed control signal from the composite signal recorded on a single DIRECT recording track has proved quite successful. Automatic tape speed control has been applied to an Ampex FR1260 tape transport used to reproduce signals recorded using the Ampex AR200 transport.

To assess the performance of the digital acquisition hardware it has also been necessary to complete the ground station digital interface hardware[13] and produce suitable software to allow the data to be read into a computer. Both NRZ and RZ forms of serial recording have been tested. Error-free recording has been demonstrated over long periods in both cases. Because the RZ recording technique requires only one track it has been adopted as the standard system of serial recording and has been more exhaustively tested than the NRZ recording format.

Parallel digital recording hardware has been completely tested with a direct connection between the airborne data processor and the ground station digital interface, but since an in-line recording head has not been available no parallel recording has been performed.

Normally the multiplexer/ADC (DSE model 480001) is operated in the auto-ranging mode. The excellent performance characteristics of this equipment have proved very advantageous where a number of transducer outputs of widely differing levels are to be encoded. Where signal filtering is required to eliminate aliasing problems when the data are reproduced, additional signal conditioning hardware will be a requirement and the major advantage of the auto-ranging multiplexer/ADC (i.e. the reduction in the amount of additional conditioning hardware required) may not then be realized. However, it is intended that digital recording will be used mainly for engine performance parameters for which anti-aliasing filtering will not, in the main be required.

The advantages associated with time-of-day recording have been clearly demonstrated. Time-of-day data have been used in conjunction with computer software to read selected blocks of data. Such a form of pre-processing allows large quantities of unwanted data to be ignored by the computer. Furthermore software has been written which allows reading of data to be resumed at exactly the point previously left off during an earlier read-in of data. A hardware interface has been arranged and suitable software has been written to allow computer

control of the analogue tape reproducing machine. With these capabilities large blocks of data can be read and processed by the computer by taking smaller manageable blocks in turn.

An analogue demultiplexer has been manufactured to allow separation of the eight channels of analogue data recorded on one tape recording track using the FM form of recording. Time-of-day and synchronizing signals derived from the ground station digital interface allow "point" or "block" sampled analogue data to be suitably separated.

Definition of the various items of airborne hardware and the associated cables which comprise the airborne acquisition system are given in Figure 29. Photographs of the major items of acquisition hardware defined are included. Details of figure numbers are given in the following table.

Item	Figure No. of photograph
Airborne data processor	30
Airborne multiplexer and analogue to digital converter (DSE model 480001)	31
Time-of-day display	32
Tape recording equipment	33
Cable adaptors	34

9. REVIEW OF DATA ACQUISITION SYSTEM

Since the time the manufacture of equipment described in this report was started many new components, both in the form of integrated circuit devices and of complete data acquisition modules, have become available commercially. With presently available components the circuit functions detailed herein could have been performed more simply and with reduced component count. Some obvious improvements which could be incorporated are:

(i) use of frequency division devices with higher division factors;
(ii) use of tri-state devices for digital multiplexing onto a common bus;
(iii) use of read-only-memory devices for pre-selection of channel sampling sequence and for range selection when the digital data acquisition system is operated in the programmed mode.

The system of using a two-bit gap for word synchronization and a frame word (with bit gaps) for frame synchronization of serial digital data guarantees that the data reduction equipment will not lose synchronization even if one word is mutilated because of tape dropout or other cause. One disadvantage of the use of time gaps for synchronization purposes is that analogue techniques (electronic flywheel in the case of the present data reduction equipment) are required to detect these gaps when the data are reproduced. It would seem that word synchronization could be dispensed with and frame synchronization only retained, particularly as there have been no observable problems with loss of synchronization with the present system.

By devoting one bit per data word plus one complete word for synchronization purposes a continuous data stream without time gaps could be used. If 16-bit words are to be encoded the minimum word length would then be 17 bits if longitudinal parity is omitted or 18 bits if longitudinal parity is included. An encoding pattern which could be used for the latter is given in Figure 35. With that pattern 18 consecutive zeros would uniquely define a new frame. Individual words in the frame could be extracted by counting 18-bit sequences from the time the new frame is detected. Such a pattern used in conjunction with the RZ encoding technique[14] would provide a data stream which could be read using purely digital techniques. Excellent immunity from the effects of tape transport speed variations would result. Such immunity would prove very advantageous if low grade tape transports (e.g. some cassette types) were used.

No serious attempt has been made with the present digital encoding system to maximize the bit packing density on magnetic tape. Increased density could be achieved by using linear (rather than saturation) recording and by using a wider bandwidth tape recorder (with reduced headgap widths).

Although the data processor has been specifically designed to control the DSE model 480001 analogue multiplexer/ADC, alternative multiplexer/ADC equipment can just as simply be used. The basic control signals provided by the data processor can be used with virtually any other similar hardware with random address selection.

In the interests of future expansion two spare printed circuit card slots have been incorporated in the data processor. Also existing circuits can be upgraded without the need to change any of the internal interwiring or output cabling.

10. CONCLUSIONS

(*a*) A tape speed reference signal can be combined with speech and recorded on a single DIRECT channel.

(*b*) Wideband analogue data can be multiplexed in blocks at a fairly low sampling rate and the composite signal recorded on a single FM channel. Time-of-day recorded together with other digital data can be used to demultiplex the data at the time of reproduction.

(*c*) A versatile system of serial digital recording of 16-bit words onto a single tape track can be readily implemented.

(*d*) Time-of-day, date and run number information can be continuously recorded using only one word per frame of data.

(*e*) An alternative encoding scheme which does not require any time gaps for synchronization purposes could be used.

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APPENDIX 1

Component Identification

Components used on printed circuits and elsewhere have been given an identification label (or legend) consisting of a letter prefix followed by a three-digit number. The letter prefix identifies the class of component as indicated in the following table.

Class of component	Letter prefix
Resistor	R
Capacitor	C
Inductor or transformer	L
Diode	CR
Transistor or integrated circuit	Q
Switch	S
Chassis mounted connector	J
Cable mounted connector or edge connector contacts on printed circuit board	P
Heat sink	HS
Crystal	Y
Test point	TP

The three-digit number following the letter prefix identifies any individual component of the particular class. Of these digits the first, in the case of printed circuits, identifies which particular board the component is on, and the remaining two identify the particular component. For example, R213 means resistor 13 on printed circuit board 2. In the case of power supply components the first digit has been omitted.

The board identifiers are marked on the board extractors (mounted on the boards) and are also marked on the corresponding card locations in the data processor box. Complete component identification labels are included on circuit diagrams and component layout diagrams. Board identifiers are allocated as indicated in the following table.

Board identifier	Board description
0	Timing Signals Generator and Modulator
1	Analogue Multiplexer Control Signal Generator
2	Analogue Multiplexer
3	Time Code Generator
4	Digital Multiplexer No. 1
5	Digital Multiplexer No. 2
6	Programmer
7	Parallel to Serial Converter
8	Spare
9	Spare

Repetition of a particular sub-circuit within an integrated circuit (e.g. dual input NAND gate is repeated four times in the SN5400) is indicated by consecutive letters following the integrated circuit identifier (e.g. if Q313 is a type SN5400 then Q313A, Q313B, Q313C and Q313D would serve to identify each sub-circuit).

Chassis mounted (i.e. front panel) switches are given a two-digit identifier only in addition to the "S" prefix.

Connectors (both cable and chassis types) are given a three-digit identifier where the first digit is a unit identifier which, for the airborne data processor, is 6. Other units of interest here are indicated in the following table together with their associated unit identifier.

Unit	Unit No.
Ampex AR200 Tape Transport	1
Ampex AR200 Electronics Unit	2
Dynamics Systems Electronics Multiplexer and Analogue to Digital Converter	5
Time Display	7

Mating plugs and sockets are always given the same number identification.

Each unit of equipment manufactured is given a serial number of the form FL-n_1n_2-n_3n_4. "FL" is an abbreviation for "FLIGHT", n_1n_2 is a two-digit project identifier and n_3n_4 is a two-digit equipment identifier. In the case of the airborne data processor the serial number is FL-01-03 where the "01" refers to the project "airborne data acquisition and ground station data reduction" and the "03" refers to the "airborne data processor".

Printed circuit boards are also given serial numbers consisting of the unit serial number followed by a particular board identification (e.g. FL-01-03-02). Boards manufactured for the data processor have serial numbers as given in the following table.

Serial number	Board description
FL-01-03-00	Extender board (for testing plug-in boards)
FL-01-03-01	Board 0, Timing Signals Generator and Modulator
FL-01-03-02	Board 1, Analogue Multiplexer Control Signal Generator
FL-01-03-03	Board 2, Analogue Multiplexer
FL-01-03-04	Board 3, Time Code Generator
FL-01-03-05	Boards 4 and 5, Digital Multiplexer
FL-01-03-06	Board 6, Programmer
FL-01-03-07	Board 7A, Parallel to Serial Converter (serial system)
FL-01-03-08	Board 7B, Parallel to Serial Converter (parallel system)
FL-01-03-09	Power Supply board A
FL-01-03-10	Power Supply board B

APPENDIX 2

Integrated Circuit Wiring Details

Any digital integrated circuit connections (including power) which are not given in the circuit diagrams are included in the following tables. Dual-in-line packages have been used throughout. The package size is indicated in each case (where 14DIL means 14 pin dual-in-line package and similarly for 16DIL).

All digital integrated circuits are mounted with a 10,000 pF power supply bypass capacitor in close proximity to the device.

Device identification		Connected to com. (gnd)	Connected to V_{CC}	Other details	Package size
Legend	Type				
Q001	SN5404	7	14		14DIL
Q002	SN5492	6, 7, 10	5	1 connected to 14	14DIL
Q003	SN5492	6, 7, 10	5		14DIL
Q004	SN5493	2, 3, 10	5	11 connected to 14	14DIL
Q005	SN5404	7	14		14DIL
Q006	SN5490	2, 3, 6, 7, 10	5	11 connected to 14	14DIL
Q007	SN5490	2, 3, 6, 7, 10	5	11 connected to 14	14DIL
Q008	SN5490	2, 3, 6, 7, 10	5	11 connected to 14	14DIL
Q009	SN5404	7	14		14DIL
Q010	SN5490	2, 3, 6, 7, 10	5		14DIL
Q011	SN5492	6, 7, 10	5		14DIL
Q012	SN5492	6, 7, 10	5	8 connected to 14	14DIL
Q013	SN5493	2, 3, 10	5	11 connected to 14	14DIL
Q014	SN5404	7	14		14DIL
Q015	SN5404	7	14		14DIL
Q101	SN5493	10	5	1 connected to 12	14DIL
Q102	SN5493	10	5		14DIL
Q103	SN5490	6, 7, 10	5		14DIL
Q104	SN5490	6, 7, 10	5	1 connected to 12	14DIL
Q105	SN5492	10	5	1 connected to 12	14DIL
Q106	SN5493	2, 3, 10	5	1 connected to 12	14DIL
Q107	SN5400	7	14		14DIL
Q108	SN5400	7	14		14DIL
Q109	SN5400	7	14		14DIL
Q110	SN5430	7	14		14DIL
Q111	SN5410	7	14		14DIL
Q112	SN5400	7	14		14DIL
Q113	SN5400	7	14		14DIL
Q114	SN5400	7	14		14DIL
Q115	SN5430	7	14		14DIL
Q116	SN5402	7	14		14DIL
Q117	SN5404	7	14		14DIL
Q118	SN5404	7	14		14DIL
Q119	SN5493	10	5		14DIL

Device identification		Connected to com. (gnd)	Connected to V_{CC}	Other details	Package size
Legend	Type				
Q201	SN5404	7	14		14DIL
Q202	SN5402	7	14		14DIL
Q301	SN5404	7	14		14DIL
Q302	SN5403	7	14		14DIL
Q303	SN54121	3, 4, 7	9, 14		14DIL
Q304	SN5476	1, 4, 12, 13, 16	5, 7		16DIL
Q305	SN5400	7	14		14DIL
Q306	SN5400	7	14		14DIL
Q307	SN54192	8	16		16DIL
Q308	SN54192	8, 9	16		16DIL
Q309	SN54192	8	16		16DIL
Q310	SN54192	8, 9	16		16DIL
Q311	SN54192	8	16		16DIL
Q312	SN54192	8, 9, 10	16		16DIL
Q313	SN5400	7	14		14DIL
Q314	SN5400	7	14		14DIL
Q315	SN5400	7	14		14DIL
Q316	SN5404	7	14		14DIL
Q317	SN5404	7	14		14DIL
Q318	SN5404	7	14		14DIL
Q501	SN54153	1, 8, 15	16		16DIL
Q502	SN54153	1, 8, 15	16		16DIL
Q503	SN54153	1, 8, 15	16		16DIL
Q504	SN54153	1, 8, 15	16		16DIL
Q505	SN54153	1, 8, 15	16		16DIL
Q506	SN54153	1, 8, 15	16		16DIL
Q507	SN54153	1, 8, 15	16		16DIL
Q508	SN54153	1, 8, 15	16		16DIL
Q601	SN5404	7	14		14DIL
Q602	SN5402	7	14		14DIL
Q603	SN5400	7	14		14DIL
Q604	SN5490	2, 3, 10	5, 6	1 connected to 12	14DIL
Q605	SN5442	8	16		16DIL
Q606	SN5476	13, 6	2, 4, 5, 9, 12, 16		16DIL
Q607	SN5404	7	14		14DIL
Q608	SN5490	2, 3, 10	5, 6	1 connected to 12	14DIL
Q609	SN5404	7	14		14DIL
Q610	SN5404	7	14		14DIL
Q611	SN5442	8	16		16DIL
Q612	SN5476	13	2, 5, 7, 9, 12, 16		16DIL
Q613	SN5493	10	3, 5	1 connected to 12	14DIL
Q614	SN5400	7	14		14DIL

Device identification		Connected to com. (gnd)	Connected to Vcc	Other details	Package size
Legend	Type				
Q615	SN5476	13	2, 4, 5, 7, 9, 12, 16		16DIL
Q616	SN5400	7	14		14DIL
Q617	SN5420	7	14		14DIL
Q618	SN5420	7	14		14DIL
Q701	SN5490	6, 7, 10	5	1 connected to 12, 2 connected to 3	14DIL
Q702	SN5402	7	14		14DIL
Q703	SN5410	7	14		14DIL
Q704	SN5404	7	14		14DIL
Q705	SN5402	7	14		14DIL
Q706	SN5400	7	14		14DIL
Q707	SN5400	7	14		14DIL
Q708	DM7590	8, 10	16		16DIL
Q709	DM7590	8	16		16DIL
Q710	SN54121	7	5, 14	3 connected to 4, R705 connected between 11 and 14, C702 connected between 10 and 11	14DIL
Q711	SN54121	7	5, 9, 14	3 connected to 4, C703 connected between 10 and 11	14DIL
Q712	SN5476	13	2, 4, 5, 7, 9, 12, 16		16DIL
Q713	SN5404	7	14		14DIL
Q714	SN5400	7	14		14DIL
Q751	SN5475	12	5		16DIL
Q752	SN5475	12	5		16DIL
Q753	SN5475	12	5		16DIL
Q754	SN5475	12	5		16DIL
Q755	SN54153	1, 8, 15	16		16DIL
Q756	SN54153	1, 8, 15	16		16DIL
Q757	SN5476	13	2, 3, 5, 7, 8		16DIL
Q758	SN5476	13	2, 3, 5, 7, 8		16DIL
Q759	SN5476	13	2, 3, 5, 7, 8		16DIL
Q760	SN5476	13	2, 3, 5, 7, 8, 9, 12		16DIL
Q761	SN5404	7	14		14DIL
Q762	SN5404	7	14		14DIL
Q763	SN5402	7	14		14DIL
Q764	DM7220	4, 5, 6, 7	14		14DIL
Q765	SN5440	7	14		14DIL

APPENDIX 3

Component Lists

The following tables list the components used in the airborne data processor. Resistance, inductance and capacitance values given in these tables (and also marked on the circuit diagrams) are respectively in ohm, microhenry and picofarad (where K = 10^3 and M = 10^6). Thus a capacitance value designated 1·5K means 1500 picofarad and a capacitance value designated 10M means 10 microfarad.

Digital integrated circuits listed in Appendix 2 have been omitted from the following tables.

3.1 Components for Board 0 (Timing Signals Generator and Modulator)

Legend	Value	Description
R001, R002	8·2K	Resistor, fixed, metal film, RL07 series.
R003	3·9K	As for R001.
R004	100	Resistor, fixed, carbon film, CR16 series.
R005	47K	As for R004.
R006	390	As for R001.
R007, R008	10K	Resistor, variable, wire-wound, Bourns type 224P-1.
R009, R010	4·7K	Resistor, fixed, glass–tin–oxide, Electrosil, style RFG-5F, type TR4.
R011	1K	As for R009.
R012	1·2K	As for R009.
R013, R014	4·7K	As for R009.
R015	1K	As for R009.
R016	1·2K	As for R009.
R017 → R030	33	As for R004.
R031	68	As for R004.
C001, C002	100K	Capacitor, fixed, ceramic, Vitramon type CK06BX104K.
C003	330K	Capacitor, fixed, Sprague, Filmite type E192.
C004	220	Capacitor, fixed, ceramic, Vitramon type VK23BW221K.
C005	460K	As for C003.
C006, C007	100K	As for C001.
C008 → C010	6·8M	Capacitor, fixed, electrolytic, tantalum, Sprague type 196D.
C011 → C025	10K	Capacitor, fixed, ceramic, Vitramon type CK06BX103K.
C026	1M	Capacitor, fixed, ceramic, Vitramon VK33BW series.
L001 → L003	27	Inductor, fixed, Cambion type 2590/30.
Y001		Quartz crystal unit, AWA type 6HAZ, 3·6000 MHz.
Y002		Quartz crystal unit, AWA type 6HAZ, 3·6864 MHz.
Q016		Integrated circuit, operational amplifier, National type 741H, 8-pin round package.
Q017		Integrated circuit, gate-controlled wideband amplifier, Motorola type MC1545G, 10-pin round package.
CR001, CR002		Diode, silicon, OA202.
CR003, CR004		Diode, zener, BZY88 series, 3·9 V.

3.2 Components for Board 1 (Analogue Multiplexer Control Signal Generator)

Legend	Value	Description
R101, R102	390	Resistor, fixed, metal film, RL07 series.
R103 → R115	220	As for R101.
C101	6·8M	Capacitor, fixed, electrolytic, tantalum, Sprague type 196D.
C102 → C105	1·5K	Capacitor, fixed, ceramic, Vitramon type VK33BW152K.
C106 → C124	10K	Capacitor, fixed, ceramic, Vitramon type CK06BX103K.
L101	27	Inductor, fixed, Cambion type 2590/30.

3.3 Components for Board 2 (Analogue Multiplexer)

Legend	Value	Legend
R201 → R203	33K	Resistor, fixed, metal film, RL07 series.
R204	30K	As for R201.
R205	5K	Resistor, variable, wire-wound, Bourns type 224P-1.
R206	270	As for R201.
C201 → C204	6·8M	Capacitor, fixed, electrolytic, tantalum, Sprague type 196D.
C205 → C220	10K	Capacitor, fixed, ceramic, Vitramon type CK06BX104K.
L201 → L203	27	Inductor, fixed, Cambion type 2590/30.
CR201		Diode, zener, 10·5 V, type 1ZC10T5.
Q203 → Q206		Integrated circuit, Dual double-pole single-throw analog switch, National type NH0019D, 14-pin dual-in-line package.
Q207		Integrated circuit, operational amplifier, National type 741H, 8-pin round package.

3.4 Components for Board 3 (Time Code Generator)

Legend	Value	Description
R301	1K	Resistor, fixed, glass-tin-oxide, Electrosil, style RFG-5F, type TR4.
R302	3·9K	Resistor, fixed, metal film, RL07 series.
R303	100	As for R302.
R304	100	Resistor, fixed, carbon film, CR16 series.
R305	51	As for R302.
R306 → R308	470	As for R301.
C301	6·8M	Capacitor, fixed, electrolytic, tantalum, Sprague type 196D.
C302 → C304	100K	Capacitor, fixed, ceramic, Vitramon type CK06BX104K.
C305 → C307	330	Capacitor, fixed, ceramic, Vitramon type VK23BW331K.
C308 → C325	10K	Capacitor, fixed, ceramic, Vitramon type CK06BX103K.
L301	27	Inductor, fixed, Cambion type 2590/30.

3.5 Components for Boards 4 and 5 (Digital Multiplexers Nos 1 and 2)

Legend	Value	Description
R501, R503 . . . R595	100	Resistor, fixed, carbon film, CR16 series.
R502, R504 . . . R596	47K	As for R501.
C501 → C548	220	Capacitor, fixed, ceramic, Vitramon type VK23BW221K.
C549	6·8M	Capacitor, fixed, electrolytic, tantalum, Sprague type 196D.
C550 → C557	10K	Capacitor, fixed, ceramic, Vitramon type VK23BW103K.
L501	27	Inductor, fixed, Cambion type 2590/30.

3.6 Components for Board 6 (Programmer)

Legend	Value	Description
R601	47K	Resistor, fixed, carbon film, CR16 series.
R602, R603	390	Resistor, fixed, glass-tin-oxide, Electrosil, style RFG-5F, type TR4.
R604 → R608	33	As for R601.
R609	47K	As for R601.
R610	100	As for R601.
R611	47K	As for R601.
R612	100	As for R601.
R613	47K	As for R601.
R614	100	As for R601.
R615	220	Resistor, fixed, metal film, RL07 series.
R616 → R625	22K	As for R615.
R626	470	As for R602.
C601	820	Capacitor, fixed, ceramic, Vitramon type VK23BW821K.
C602	1K	Capacitor, fixed, ceramic, Vitramon type VK23BW102K.
C603	1·5K	Capacitor, fixed, ceramic, Vitramon type VK23BW152K.
C604 → C607	220	Capacitor, fixed, ceramic, Vitramon type VK23BW221K.
C608	820	As for C601.
C609	1·5K	As for C603.
C610	1K	As for C602.
C611	6·8M	Capacitor, fixed, electrolytic, tantalum, Sprague type 196D.
C612 → C629	10K	Capacitor, fixed, ceramic, Vitramon type CK06BX103K. or type VK23BW103K.
C630	2·2K	Capacitor, fixed, ceramic, Vitramon VK23BW222K.
L601	27	Inductor, fixed, Cambion type 2590/30.
TP1 → TP5		Test point, Amp series 3-582118.

3.7 Components for Board 7A (Parallel to Serial Converter—Serial System)

Legend	Value	Description
R701	100	Resistor, fixed, carbon film, CR16 series.
R702	33	As for R701.
R703	47K	As for R701.
R704	10K	Resistor, fixed, glass-tin-oxide, Electrosil, style RFG-5F, type TR4.
R705, R706	390	As for R704.
R707, R708	33	As for R701.
R709	390	As for R704.
R710	10K	As for R704.
R711	1·8K	As for R704.
R712	47K	As for R701.
R713	4·7K	As for R704.
R714	2·2K	As for R704.
R715	8·2K	Resistor, fixed, metal film, RL07 series.
R716	10K	As for R704.
R717	1·8K	As for R704.
R718	47K	As for R701.
R719 → R722	1K	As for R704.
R723	2·2K	As for R704.
R724	330	As for R704.
R725, R726	33	As for R701.
C701	220	Capacitor, fixed, ceramic, Vitramon type VK23BW221K.
C702, C703	680	Capacitor, fixed, ceramic, Vitramon type VK23BW681K.
C704 → C706	820	Capacitor, fixed, ceramic, Vitramon type VK23BW821K.
C707	6·8M	Capacitor, fixed, electrolytic, tantalum, Sprague type 196D.
C708, C709	10K	Capacitor, fixed, ceramic, Vitramon type VK23BW103K.
C710, C711	6·8M	As for C707.
C712 → C725	10K	Capacitor, fixed, ceramic, Vitramon type CK06BX103K.
L701	27	Inductor, fixed, Cambion type 2590/39.
TP1 → TP4		Test point, Amp series 3-582118.
Q715, Q716		Transistor, silicon, NPN, type AY6101.
Q717, Q718		Transistor, silicon, PNP, type AY6102.

3.8 Components for Board 7B (Parallel to Serial Converter Parallel System)

Legend	Value	Description
R751 → R759	33	Resistor, fixed, carbon film, CR16 series.
R760, R761	470	Resistor, fixed, glass-tin-oxide, Electrosil, style RFG-5F, type TR4.
C751, C752	1·5K	Capacitor, fixed, ceramic, Vitramon type VK23BW152K.
C753	820	Capacitor, fixed, ceramic, Vitramon type VK23BW821K.
C754	6·8M	Capacitor, fixed, electrolytic, tantalum, Sprague type 196D.
C755 → C769	10K	Capacitor, fixed, ceramic, Vitramon type CK06BX103K.
L751	27	Inductor, fixed, Cambion type 2590/30.

3.9 Components for Power Supply

Legend	Value	Description
R01	10K	Resistor, fixed, glass-tin-oxide, Electrosil, style RFG-5F, type TR4.
R02	82	As for R01.
R03	47	As for R01.
R04	82	As for R01.
R05, R06	0·1	Resistor, fixed, wire-wound, Welwyn W21 series, 5%, 3 W.
R07	560	As for R01.
R08	2·7K	As for R01.
R09	8·2K	As for R01.
R10	100	As for R01.
R	0·074	Printed circuit allows up to three Welwyn W21 series resistors (as for R05) to be connected in parallel to make up this value.
R12	3·6K	As for R01.
R13	1K	Resistor, variable, wire-wound, Bourns type 224P-1.
R14	510	As for R01.
R15	1·2K	As for R01.
R16	0·1	As for R05.
R17	2·7	As for R05.
R18	16K	As for R01.
R19	1K	As for R13.
R20	1·2K	As for R01.
R21	820	As for R01.
R22	0·1	As for R05.
R23	4·7	As for R05.
R24		Two resistors in parallel as for R01, value to be selected to give −15 V output.
C01, C02	100K	Capacitor, fixed, ceramic, Vitramon type VK30BX104K.
C03	6·8M	Capacitor, fixed, electrolytic, tantalum, Sprague type 196D.
C04	100K	As for C01.
C05	50M	Capacitor, fixed, electrolytic, tantalum, Sprague type 125.
C06, C07	300M	Capacitor, fixed, electrolytic, tantalum, Sprague type 109D.
C08, C09	100K	As for C01.
C10, C11	300M	As for C06.
C12, C13	100K	As for C01.
C14	27K	Capacitor, fixed, ceramic, Vitramon type VK30BX273K.
C15		As for C01, value to be selected to guarantee circuit stability.
C16	50M	As for C05.
C17	100K	As for C01.
C18	27K	As for C14.
C19		As for C01, value to be selected to guarantee circuit stability.
C20	6·8M	As for C03.
C21	100K	As for C01.
C22	50M	As for C05.
C23	100K	As for C01.
C24	6·8M	As for C03.
C25	100K	As for C01.
L01	30K	Inductor, specially wound on Telcon type 2C 0·002 inch HCR tape wound toroidal core, winding 148 turns 21B&S

Legend	Value	Description
L02		Transformer. Winding No.* / Symbol for no. of turns / Wire size 1 / N3 - N3 / 21 - 21 turns using two 18 B&S wires in parallel. 2 / N4 / 46 turns, 30 B&S. 3 / N5 / 46 turns, 30 B&S. 4 / N1 - N1 (bifilar) / 44 - 44 turns using two 18 B&S wires in parallel for each winding. 5 / N2 - N2 (bifilar) / 57 - 57 turns, 33 B&S. * Winding 1 closest to core and so on progressively. Shield is placed between winding No. 3 and winding No. 4.
CR01		Diode, silicon, type OA202.
CR02		Diode, silicon, Motorola type 1N4003.
CR03		As for CR02.
CR04		Diode, silicon, Mullard type BYX48-900R.
CR05		As for CR04.
CR06		Diode, zener, 18·5 V, type 1Z18T5.
CR07		Diode, regulator, 2·4 V, type LM103.
CR08		Rectifier bridge assembly, Motorola type MDA942-2.
CR09		As for CR08.
Q01, Q02		Transistor, silicon, PNP, type 2N3792.
Q03, Q04		Darlington transistor device, PNP, type MJ901.
Q05		Integrated circuit, voltage regulator, type LM105H, 8-pin round package.
Q06		Transistor, silicon, PNP, type 2N5195.
Q07		As for Q05.
Q08		Integrated circuit, voltage regulator, type LM104H, 10-pin round package.
Q09		As for Q06.
HS01		Heat sink, specially manufactured (area at least 36 sq. in.).
HS02, HS03		Heat sink, specially manufactured utilizing two Redpoint type CH77 heatsinks.
TP1 → TP5		Test point, Amp series 3-582118.
J620		Socket, chassis, printed circuit edge mounting, 50 pin per side, Elco type 6309-050-298-001.
J621		Socket, chassis mounted, Souriau type 8140-01.
J622		Plug, chassis mounted, Souriau type 8140-26 (incorporating biasing socket in place of pin 1).

3.10 Components for Front Panel and Chassis

Legend	Description
S1A, S1B, S1C, S1D	Switch, 10 position thumbwheel, 4-line BCD output, Contraves type SM140.
S2A	As for S1A, movement restricted to position 0 and 1, Contraves type SM140/A01.
S2B	As for S1A.
S2C	As for S1A, movement restricted to positions 0 to 3, Contraves type SM140/A03.
S2D	As for S1A.
S3	Switch, pushbutton, double-pole (but one pole only used), change-over, momentary make, Alco type MSP205R.
S4	As for S3.
S5A	As for S1A, movement restricted to positions 0 to 2, Contraves type SM140/A02.
S5B	As for S1A.
S5C	As for S1A, movement restricted to positions 0 to 5, Contraves type type SM140/A05.
S5D	As for S1A.
S5E	As for S5C.
S5F	As for S1A.
S6	Switch, toggle, single pole, changeover, C&K type 7101.
S7	As for S3.
S8A, 28B	Switch, 10 position thumbwheel, single-pole, Contraves type S010.
S8C	As for S8A, movement restricted to positions 0 to 3, Contraves type S010/A03.
S9	As for S6.
S10	Switch, 11-position thumbwheel, single-pole, Contraves type S011.
S11	As for S8A, movement restricted to positions 0 to 6, Contraves type S010/A06.
S12	As for S8A, movement restricted to positions 0 to 5, Contraves type type S010/A05.
S13	As for S10.
J601	Plug, chassis, Cannon type KPT02-E-8-4P.
J602	Plug, chassis, Cannon type TM-R575N.
J603	Socket, chassis, Cannon type KPT02-E-16-26S.
J604, J605	Plug, chassis, Cannon type KPT02-E-14-19P.
J606	Socket, chassis, Cannon type KPT02-E-14-18S.
J607	Plug, chassis, Cannon type KPT02-E-18-32PY.
J608	Plug, chassis, Cannon type KPT02-E-18-32PW.
J609	Socket, chassis, Cannon type KPT02-E-18-32SX.
J610 → J619	Socket, chassis, printed circuit edge mounting, 50 pin per side, Elco type 6309-050-298-001.
P621	Plug, cable mounted, Souriau type 8140-02.
P622	Socket, cable mounted, Souriau type 8140-25 (incorporating biasing pin in place of socket pin 1).
J631 → J651	Socket, printed circuit edge mounting, 12-contact, supplied by Contraves for use with their thumbwheel switches.

APPENDIX 4

Interwiring Details

Details of all interwiring connections within the data processor unit are included (or referred to) in this Appendix.

A summary of the data processor connectors together with their application is given in the following table. Details on the types of connectors and switches (referred to in this Appendix) are given in Appendix 3.10.

Connector	Location	Application
J601	Front panel	Power input.
J602	Front panel	Speech input.
J603	Front panel	Output for analogue tape recorder.
J604	Front panel	Digital transducer input No. 1.
J605	Front panel	Digital transducer input No. 2.
J606	Front panel	Control output for multiplexer and ADC.
J607	Front panel	Data processor analogue multiplexer input.
J608	Front panel	Digital input from ADC.
J609	Front panel	Output for time-of-day display.
J610	Internal sub-chassis	Board 0 (Timing Signals Generator and Modulator, edge connector.
J611	Internal sub-chassis	Board 1 (Analogue Multiplexer Control Signal Generator), edge connector.
J612	Internal sub-chassis	Board 2 (Analogue Multiplexer), edge connector.
J613	Internal sub-chassis	Board 3 (Time Code Generator), edge connector.
J614	Internal sub-chassis	Board 4 (Digital Multiplexer No. 1), edge connector.
J615	Internal sub-chassis	Board 5 (Digital Multiplexer No. 2), edge connector.
J616	Internal sub-chassis	Board 6 (Programmer), edge connector.
J617	Internal sub-chassis	Board 7 (A or B) (Parallel to Serial Converter), connector.
J618	Internal sub-chassis	Spare board connector.
J619	Internal sub-chassis	Spare board connector.
J631 → J651	Behind front panel thumbwheel switches	Thumbwheel switch connectors (Fig. 28).
P621	At end of flexible cable	Internal regulated power input (connected to power supply output).
P622	At end of flexible cable	Internal power output (connected to power supply input).

4.1 Power Distribution

Input power is derived from a 28 V (nominal) supply via front panel connector J601 wired as indicated in the following table.

J601 WIRING

Pin	Connected to	Signal description
A	P622-4, J609-Y	+ 28 V (nominal) input
B	P622-2, J609-X	28 V return (input ground)
C	Chassis lug in data processor case, J622-5	Data processor case ground
D	Adjacent J601-C pin	External cable shield

P622 is attached to a flexible cable which couples to J622 in the power supply (Fig. 24). Wiring information for P622 is given in the following table.

P622 WIRING

Pin	Connected to	Signal description
1	Used for biasing pin	
2	J601-B	28 V return
3		
4	J601-A	+ 28 V (nominal)
5	J601-C	Power supply case ground

Wiring to connectors J620, J621 and J622 which are mounted on the power supply unit (Section 7) has been indicated in Figure 24.

P621 plugs into J621 which is coupled to the regulated outputs from the power supply. Power is transferred to the data processor circuits via P621 for which wiring details are given in the following table. Only the main heavy current connections are indicated. Separate lines for each connection point indicated in the following table are not coupled back to P621; heavy duty lines are sequentially coupled from one printed circuit board edge connector to the next. Further (low current) connections are indicated elsewhere in this Appendix.

P621 WIRING
(heavy current lines only)

Pin	Connected to	Signal description
1	J610 48b, J611 48b, J612 48b, J613 48b, J614 48b, J615 48b, J616 48b, J617 48b, J618 48b, J619 48b.	15 V output
2	J610 46b, J611 46b, J612 46b, J613 46b, J614 46b, J615 46b, J616 46b, J617 46b, J618 46b, J619 46b.	Analog common
3	J610 44b, J611 44b, J612 44b, J613 44b, J614 44b, J615 44b, J616 44b, J617 44b, J618 44b, J619 44b.	15 V output
4	J610 1a, J610 1b, J610 50a, J610 50b, J611 1a, J611 1b, J611 50a, J611 50b, J612 1a, J612 1b, J612 50a J612 50b, J613 1a, J613 1b, J613 50a, J613 50b, J614 1a, J614 1b, J614 50a, J614 50b, J615 1a, J615 1b, J615 50a, J615 50b, J616 1a, J616 1b, J616 50a, J616 50b, J617 1a, J617 1b, J617 50a, J617 50b, J618 1a, J618 1b, J618 50a, J618 50b, J619 1a, J619 1b, J619 50a, J619 50b.	Digital common
5	J610 10b, J610 41b, J611 10b, J611 41b, J612 10b, J612 41b, J613 10b, J613 41b, J614 10b, J614 41b, J615 10b, J615 41b, J616 10b, J616 41b, J617 10b, J617 41b, J618 10b, J618 41b, J619 41b.	5 V output

4.2 Wiring to Front Panel Mounted Switches

Circuit information and interwiring details for front panel mounted switches S1 to S13 are given in Figure 28. The thumbwheel switches engage with 12-pin sockets J631 to J651 indicated in that figure.

4.3 Wiring to Front Panel Mounted Connectors

Lists of wiring connections to the front panel mounted connectors J602 to J609 are included here together with descriptive information for the inputs and the outputs. Wiring details for the front panel mounted power input connector J601 have been given in Appendix 4.1.

Unless otherwise specified all the wiring is unshielded.

(*a*) Wiring to J602 (speech input).

Pin	Connected to	Signal description
1	J610 46b.	Speech low
2	J610 47b.	Speech high
Body	Mounted directly on chassis and connected to internal cable shield.*	

* Shielded twisted pair wire W1 (defined in Appendix 5.2) is used with white wire to pin 2 and black wire to pin 1. The shield is left unconnected near J610.

(*b*) Wiring to J603 (output for analogue tape recorder).

Pin	Connected to	Signal description
A	J610 4b	DIR output
B	J610 46b	Common for DIR output
C	J612 7b	FM output
D	J612 8b	Common for FM output
E	J617 4a	RZ output
F	J617 3a	Common for RZ output
G	J617 9a	NRZ1 output
H	J617 8a	Common for NRZ1 output
J	J617 12a	NRZ2 output
K	J617 11a	Common for NRZ2 output
L	J617 25a	NRZ3 output
M	J617 24a	Common for NRZ3 output
N	J617 28a	NRZ4 output
P	J617 27a	Common for NRZ4 output
R		
S		
T	J617 38a	NRZ5 output
U	J617 37a	Common for NRZ5 output
V	J617 43a	NRZ6 output
W	J617 42a	Common for NRZ6 output
X	J617 45a	NRZ7 output
Y	J617 44a	Common for NRZ7 output
Z		
a		
b		
c		

Shielded wire W3 (defined in Appendix 5.2) is used with the shields forming the "common" connections in each case.

(c) Wiring to J604 (digital transducer input No. 1).

Pin	Connected to	Signal description
A	J615 10a	Bit 0 (most significant bit)
B	J615 6b	Bit 1
C	J615 8a	Bit 2
D	J615 2a	Bit 3
E	J615 20a	Bit 4
F	J615 15a	Bit 5
G	J615 20b	Bit 6
H	J615 17b	Bit 7
J	J615 30b	Bit 8
K	J615 24b	Bit 9
L	J615 32a	Bit 10
M	J615 37a	Common
N		
P	J615 25a	Bit 11
R	J615 42b	Bit 12
S	J615 34b	Bit 13
T	J615 45a	Bit 14
U		
V	J615 35a	Bit 15

(d) Wiring to J605 (digital transducer input No. 2).

Pin	Connected to	Signal description
A	J615 11a	Bit 0 (most significant bit)
B	J615 4b	Bit 1
C	J615 5a	Bit 2
D	J615 3a	Bit 3
E	J615 21a	Bit 4
F	J615 15b	Bit 5
G	J615 16b	Bit 6
H	J615 13b	Bit 7
J	J615 27b	Bit 8
K	J615 26b	Bit 9
L	J615 27a	Bit 10
M	J615 38a	Common
N		
P	J615 24a	Bit 11
R	J615 40b	Bit 12
S	J615 36b	Bit 13
T	J615 41a	Bit 14
U		
V	J615 40a	Bit 15

(e) Wiring to J606 (control output for multiplexer and ADC).

Pin	Connected to	Signal description
A	J617 47a	Command to convert (CTC).
B	J616 1a	Random sequential control.
C	S9 2	Auto/programmed range control.
D	J616 3b	Gain range control "1" (PR1).
E	J616 2b	Gain range control "2" (PR2).
F	J616 14b	Gain range control "4" (PR3).
G	J616 18b	Gain range control "8" (PR4).
H	J616 1b, J606 S	Common.
J	J618 41b	+ 5 V
K	J617 35b	Reset.
L	J616 35b	Multiplexer control "1" (m_0).
M	J616 36b	Multiplexer control "2" (m_1).
N	J616 27b	Multiplexer control "4" (m_2).
P	J616 34b	Multiplexer control "8" (m_3).
R	J616 33a	Multiplexer control "16" (m_4).
S	J606 H, J606 T	Common.
T	J606 S	Common.
U	Chassis lug in data processor case	Multiplexer-ADC chassis.

(*f*) Wiring to J607 (data processor analogue input).

Pin	Connected to	Signal description
A	Input 0 cable shield	Input 0 shield
B	J612 37b	Input 1 high
C	Input 1 cable shield	Input 1 shield
D	J612 34b	Input 2 high
E	Input 2 cable shield	Input 2 shield
F	J612 33b	Input 3 high
G	Input 3 cable shield	Input 3 shield
H	J612 30b	Input 4 high
J	Input 4 cable shield	Input 4 shield
K	J612 29b	Input 5 high
L	Input 5 cable shield	Input 5 shield
M	J612 26b	Input 6 high
N	Input 6 cable shield	Input 6 shield
P	J612 25b	Input 7 high
R	Input 7 cable shield	Input 7 shield
S		
T	J612 38b	Input 0 high
U	J612 38a	Input 0 low
V	J612 37a	Input 1 low
W	J612 34a	Input 2 low
X		
Y	J612 33a	Input 3 low
Z	J612 30a	Input 4 low
a	J612 29a	Input 5 low
b		
c	J612 26a	Input 6 low
d	J612 25a	Input 7 low
e		
f		
g		
h		
j		

Shielded twisted pair wire W1 (defined in Appendix 5.2) is used with white wire to "high" and black wire to "low". Shields are left unconnected near J612.

(g) Wiring to J608 (digital input from ADC).

Pin	Connected to	Signal description
A	J616 4a	ADC Bit 0 (range "8")
B	J616 3a	ADC Bit 1 (range "4")
C	J616 1a	Common
D	J615 16a	ADC Bit 4 (sign)
E	J615 14a	ADC Bit 5 (MSB)
F	J615 39a	Common
G	J615 31b	ADC Bit 8
H	J615 25b	ADC Bit 9
J	J615 47a	Common
K		
L	J615 37b	ADC Bit 12
M	J615 35b	ADC Bit 13
N	J615 48a	Common
P	J616 10a	CLK
R	J616 11a	Gate
S	J615 12a	Common
T	Chassis lug in data processor case	Multiplexer/ADC chassis
U	J615 9a	ADC Bit 2 (range "2")
V	J615 4a	ADC Bit 3 (range "1")
W		
X	J615 21b	ADC Bit 6
Y	J615 14b	ADC Bit 7
Z	J615 31a	ADC Bit 10
a	J615 26a	ADC Bit 11
b	J615 46a	ADC Bit 14
c	J615 36a	ADC Bit 15 (LSB)
d		
e	J616 5a	Over-range
f		
g		
h		
I		

(*h*) Wiring to J609 (output for time of day display).

Pin	Connected to	Signal description
A	J613—32b	1-line seconds, units
B	J613—33b	2-line seconds, units
C	J613—35b	4-line seconds, units
D	J613—31b	8-line seconds, units
E	J613—24b	1-line seconds, tens
F	J613—23b	2-line seconds, tens
G	J613—25b	4-line seconds, tens
H	J613—21b	1-line minutes, units
J	J613—17a	2-line minutes, units
K	J613—22b	4-line minutes, units
L	J613—19b	8-line minutes, units
M	J613—13a	1-line minutes, tens
N	J613—15a	2-line minutes, tens
P	J613—16a	4-line minutes, tens
R	J613—9a	1-line hours, units
S	J613—10a	2-line hours, units
T	J613—6a	4-line hours, units
U	J613—7a	8-line hours, units
V	J613—3a	1-line hours, tens
W	J613—5a	2-line hours, tens
X	J601—B	28 V return
Y	J601—A	+ 28 V (nominal) input
Z	Chassis lug in data processor case	Time display case ground
a	Chassis lug in data processor case	Power cable shield
b	J613—1b, J609—c	Common
c	J609—b, J609—d	Common
d	J609—c, J609—e	Common
e	J609—d, J609—f	Common
f	J609—e, J609—g	Common
g	J609—f, J613—50b	Common
h	J610—3b	PDM clock
j	J610—1b	Common for PDM clock

4.4 Wiring to Printed Circuit Board Edge Connectors

Lists of all wiring connections to the printed circuit edge connectors J610 to J619 are included, but in these cases descriptive information for the inputs and outputs is not added.

Power supply wiring only is taken to J608 and J609 (only eight of the available ten card spaces used at this time). These are available for future expansion if required.

Connector pins which engage with printed circuit board edge tracks on the component side are given an "a" identification and those on the other side are given a "b" identification.

(*a*) Wiring to J610.

Board 0 (Timing Signals Generator and Modulator) edge connector.

Pin No.	Connected to	Pin No.	Connected to
1a	J610—1b, J610—50a	1b	J610—1a, J611—1a, J609—j
2a		2b	
3a		3b	J609—h
4a		4b	J603—A
5a		5b	J649—9
6a		6b	
7a		7b	
8a		8b	J649—8
9a		9b	
10a		10b	J610—41b
11a		11b	J649—7
12a		12b	
13a		13b	J611—4b
14a		14b	
15a		15b	J649—4
16a		16b	
17a		17b	
18a		18b	J649—3
19a		19b	
20a		20b	J649—2
21a		21b	
22a		22b	
23a		23b	J650—2
24a		24b	
25a		25b	J650—3
26a		26b	
27a		27b	
28a		28b	J650—4
29a		29b	
30a		30b	J659—5
31a		31b	
32a		32b	
33a		33b	J650—7
34a		34b	
35a		35b	J650—8
36a		36b	
37a		37b	
38a		38b	
39a		39b	
40a		40b	
41a		41b	J611—10b, J610—41b
42a		42b	
43a		43b	
44a		44b	J611—44b
45a		45b	J650—6
46a		46b	J611—46b, J602—1, J603—B
47a		47b	J602—2
48a		48b	J611—48b
49a		49b	
50a	J610—50b, J610—1a	50b	J610—50a, J611—50a

(*b*) Wiring to J611.

Board 1 (Analogue Multiplexer Control Signal Generator) edge connector.

Pin No.	Connected to	Pin No.	Connected to
1a	J610 1b, J611 1b, J611 50a	1b	J611 1a, J612 1a
2a		2b	
3a		3b	J649 5
4a		4b	J610 13b
5a		5b	J613 48a
6a		6b	J613 44a
7a		7b	J613 28b
8a		8b	J613 32a
9a		9b	J612 5b
10a		10b	J611 41b
11a		11b	J612 4b
12a		12b	J612 3b
13a		13b	J613 39a
14a		14b	
15a		15b	
16a		16b	
17a		17b	
18a		18b	
19a		19b	
20a		20b	J651 1
21a		21b	
22a		22b	J651 2
23a		23b	
24a		24b	J651 3
25a		25b	
26a		26b	J651 4
27a		27b	
28a		28b	J651 5
29a		29b	
30a		30b	J651 7
31a		31b	
32a		32b	J651 8
33a		33b	
34a		34b	J651 9
35a		35b	
36a		36b	J651 10
37a		37b	
38a		38b	J651 11
39a		39b	
40a		40b	J651 12
41a		41b	J610 41b, J612 41b, J611 10b, J651 6
42a	J616 22b	42b	
43a		43b	
44a	J617 36b	44b	J610 44b, J612 44b
45a		45b	
46a	J617 34b	46b	J610 46b, J612 46b
47a		47b	
48a	J617 23b	48b	J610 48b, J612 48b
48a		49b	
50a	J610 50b, J611 50b, J611 1a	50b	J611 50a, J612 50a

(c) Wiring to J612.

Board 2 (Analogue Multiplexer) edge connector.

Pin No.	Connected to	Pin No.	Connected to
1a	J611—1b, J612—1b, J612—50a	1b	J612—1a, J613—1a
2a		2b	
3a		3b	J611—12b
4a		4b	J611—11b
5a		5b	J611—9b
6a		6b	
7a		7b	J603—C
8a		8b	J603—D
9a		9b	
10a		10b	J612—41b
11a		11b	
12a		12b	
13a		13b	
14a		14b	
15a		15b	
16a		16b	
17a		17b	
18a		18b	
19a		19b	
20a		20b	
21a		21b	
22a		22b	
23a		23b	
24a		24b	
25a	J607—d	25b	J607—P
26a	J607—c	26b	J607—M
27a		27b	
28a		28b	
29a	J607—a	29b	J607—K
30a	J607—Z	30b	J607—H
31a		31b	
32a		32b	
33a	J607—Y	33b	J607—F
34a	J607—W	34b	J607—D
35a		35b	
36a		36b	
37a	J607—V	37b	J607—B
38a	J607—U	38b	J607—T
39a		39b	
40a		40b	
41a		41b	J611—41b, J613—41b, J612—10b
42a		42b	
43a		43b	
44a		44b	J611—44b, J613—44b
45a		45b	
46a		46b	J611—46b, J613—46b
47a		47b	
48a		48b	J611—48b, J613—48b
49a		49b	
50a	J611—50b, J612—50b, J612—1a	50b	J612—50a, J613—50a

(*d*) Wiring to J613.

Board 3 (Time Code Generator) edge connector.

Pin No.	Connected to	Pin No.	Connected to
1a	J612 1b, J613 1b, J613 50a	1b	J613 1a, J614 1a, J609 b
2a	S7 2	2b	J614 6a
3a	J609 V	3b	J614 7a
4a		4b	J639 9
5a	J609 W	5b	J639 5
6a	J609 T	6b	J640 6
7a	J609 U	7b	J640 8
8a	J640 5	8b	J614 19a
9a	J609 R	9b	J614 17a
10a	J609 S	10b	J613 41b
11a		11b	J614 18b
12a		12b	J614 23a
13a	J609 M	13b	J640 9
14a		14b	
15a	J609 N	15b	
16a	J609 P	16b	
17a	J609 J	17b	
18a		18b	J614 9a
19a	J641 5	19b	J609 L
20a	J641 9	20b	
21a		21b	J609 H
22a	J641 6	22b	J609 K
23a	J614 4a	23b	J609 F
24a		24b	J609 E
25a	J614 16a	25b	J609 G
26a		26b	J642 5
27a		27b	J614 26a
28a	J642 8	28b	J611 7b
29a	J642 6	29b	J614 31a
30a	J614 14a	30b	J643 9
31a	J614 21b	31b	J609 D
32a	J611 8b	32b	J609 A
33a	J614 31b	33b	J609 B
34a	J614 14b	34b	J616 39b
35a	J642 9	35b	J609 C
36a	J643 5	36b	J616 38b
37a	J643 6	37b	J644 5
38a	J614 25b	38b	J614 36a
39a	J611 13b	39b	J614 46a
40a	J644 6	40b	J644 9
41a	J644 8	41b	J612 41b, J614 41b, J613 10b, J639 7
42a	J614 35b	42b	
43a	J614 37b	43b	
44a	J611 6b	44b	J612 44b, J614 44b
45a	S3 2	45b	
46a	J616 40b	46b	J612 46b, J614 46b
47a	S6 2	47b	
48a	J611 5b	48b	J612 48b, J614 48b
49a	S4 2	49b	
50a	J612 50b, J613 50b, J613 1a, J639 4	50b	J613 50a, J614 50a, J609 g

(c) Wiring to J614.

Board 4 (Digital Multiplexer No. 1) edge connector.

Pin No.	Connected to	Pin No.	Connected to
1a	J613 1b, J614 1b, J614 50a	1b	J614 1a, J615—1a, J614 3b
2a	J636 8	2b	J615 7b
3a		3b	J614 1b, J614 5b
4a	J613 23a	4b	J614 7b
5a		5b	J614 3b, J614 6b
6a	J613 2b	6b	J614 5b, J614 9b
7a	J613 3b	7b	J614 10a, J614—4b
8a	J635 5	8b	J615 9b
9a	J613 18b	9b	J614—6b
10a	J614 11a, J614 7b, J614 10b	10b	J614 41b, J614—10a
11a	J614 10a	11b	J615—6a
12a		12b	J615 7a
13a	J615 17a	13b	
14a	J613 30a	14b	J613 34a
15a	J636 9	15b	
16a	J613 25a	16b	
17a	J613 9b	17b	
18a	J615 19a	18b	J613 11b
19a	J613 8b	19b	J615 23a
20a	J636 6	20b	J636 5
21a		21b	J613 31a
22a	J615 18b	22b	J637 5
23a	J613 12b	23b	J615 22b
24a	J633 5	24b	J631 6
25a	J631 5	25b	J631 38a
26a	J613 27b	26b	J633 6
27a	J633 9	27b	J633 8
28a	J615 32b	28b	J637 9
29a	J638 8	29b	J615 28b
30a	J615 29a	30b	J631 8
31a	J613 29b	31b	J613 33a
32a	J631 9	32b	J638—6
33a	J615 33b	33b	J638 5
34a		34b	J632 6
35a	J632 5	35b	J613—42a
36a	J613 38b	36b	J634 6
37a		37b	J613 43a
38a		38b	J615 39b
39a		39b	J638 9
40a	J634 5	40b	J634 8
41a	J634 9	41b	J613—41b, J615 41b, J614—10b, J631 7, J614 11a
42a		42b	J632 8
43a	J615 42a	43b	
44a	J615 34a	44b	J613 44b, J615 44b
45a	J632 9	45b	
46a	J613 39b	46b	J613 46b, J615 46b
47a		47b	J616 5b
48a		48b	J613 48b, J615 48b
49a		49b	J616 4b
50a	J613 50b, J614 50b, J614 1a	50b	J614 50a, J615 50a, J631 4

(7) Wiring to J615.

Board 5 (Digital Multiplexer No. 2) edge connector

Pin No	Connected to	Pin No	Connected to
1a	J614 1b, J615 1b, J615 50a	1b	J615 1a, J616 1a
2a	J604 D	2b	J617 14b
3a	J605 D	3b	J616 7b
4a	J608 V	4b	J605 B
5a	J605 C	5b	J616 6b
6a	J614 11b	6b	J604 B
7a	J614 12b	7b	J614 2b
8a	J604 C	8b	J617 13b
9a	J608 U	9b	J614 8b
10a	J604 A	10b	J615 41b
11a	J605 A	11b	J617 16b
12a	J608 S	12b	J617 15b
13a	J617 5b	13b	J605 H
14a	J608 E	14b	J608 Y
15a	J604 F	15b	J605 F
16a	J608 D	16b	J605 G
17a	J614 13a	17b	J604 H
18a	J617 4b	18b	J614 22a
19a	J614 18a	19b	J617 6b
20a	J604 E	20b	J604 G
21a	J605 E	21b	J608 X
22a	J617 7b	22b	J614 23b
23a	J614 19b	23b	J617 30b
24a	J605 P	24b	J604 K
25a	J604 P	25b	J608 H
26a	J608 a	26b	J605 K
27a	J605 L	27b	J605 J
28a	J617 32b	28b	J614 29b
29a	J614 30a	29b	J617 29b
30a	J617 31b	30b	J604 J
31a	J608 Z	31b	J608 G
32a	J604 L	32b	J614 28a
33a	J617 20b	33b	J614 33a
34a	J614 44a	34b	J604 S
35a	J604 V	35b	J608 M
36a	J608 c	36b	J605 S
37a	J604 M	37b	J608 I
38a	J605 M	38b	J617 19b
39a	J608 F	39b	J614 38b
40a	J605 V	40b	J605 R
41a	J605 T	41b	J614 41b, J616 41b, J615 10b
42a	J614 43a	42b	J604 R
43a	J617 21b	43b	
44a	J617 22b	44b	J614 44b, J616 44b
45a	J604 T	45b	
46a	J608 b	46b	J614 46b, J616 46b
47a	J608 J	47b	J616 21a
48a	J608 N	48b	J614 48b, J616 48b
49a		49b	J616 19b
50a	J614 50b, J615 50b, J615 1a	50b	J615 50a, J616 50a

(g) Wiring to J616.

Board 6 (Programmer) edge connector.

Pin No.	Connected to	Pin No.	Connected to
1a	J615 – 1b, J616 – 1b, J616 – 50a, J606 – B, J608 – C	1b	J616 – 1a, J617 – 1a, J606 – H
2a	S9 – 2	2b	J606 – E
3a	J608 – B	3b	J606 – D
4a	J608 – A	4b	J614 – 49b
5a	J608 – e	5b	J614 – 47b
6a		6b	J615 – 5b
7a	J648 – 4	7b	J615 – 3b
8a		8b	J648 – 2
9a		9b	J648 – 11
10a	J608 – P	10b	J616 – 41b
11a	J608 – R	11b	
12a	J648 – 3	12b	
13a		13b	J648 – 8
14a		14b	J606 – F
15a	J648 – 12	15b	J648 – 9
16a		16b	J648 – 7
17a	J648 – 10	17b	J648 – 5
18a	J647 – 4	18b	J606 – G
19a	J647 – 3	19b	J615 – 49b
20a	J647 – 2	20b	
21a	J615 – 47b	21b	
22a		22b	J617 – 39b, J611 – 42a
23a		23b	J617 – 17b
24a		24b	J647 – 6
25a		25b	J647 – 5
26a		26b	J645 – 6
27a		27b	J606 – N
28a		28b	J646 – 6
29a		29b	
30a		30b	
31a		31b	
32a		32b	
33a	J606 – R	33b	J617 – 18b
34a	J645 – 10	34b	J606 – P
35a	J645 – 11	35b	J606 – L
36a	J645 – 12	36b	J606 – M
37a	J645 – 9	37b	J617 – 3b
38a	J645 – 8	38b	J613 – 36b
39a	J645 – 7	39b	J613 – 34b
40a	J645 – 5	40b	J613 – 46a
41a	J645 – 4	41b	J615 – 41b, J617 – 41b, J616 – 10b, S9 – 1
42a	J645 – 3	42b	
43a	J645 – 2	43b	J646 – 9
44a	J646 – 10	44b	J615 – 44b, J617 – 44b
45a	J646 – 11	45b	J646 – 8
46a	J646 – 12	46b	J615 – 46b, J617 – 46b
47a	J646 – 4	47b	J646 – 7
48a	J646 – 3	48b	J615 – 48b, J617 – 48b
49a	J646 – 2	49b	J646 – 5
50a	J615 – 50b, J616 – 50b, J616 – 1a	50b	J616 – 50a, J617 – 50a, J648 – 6

(b) Wiring to J617.

Board 7A or 7B (Parallel to Serial Converter) edge connector

Pin No.	Connected to
1a	J616 1b, J617 1b, J617 50a
2a	
3a	J603 F
4a	J603 I
5a	
6a	
7a	
8a	J603 H
9a	J603 G
10a	
11a	J603 K
12a	J603 J
13a	
14a	
15a	
16a	
17a	
18a	
19a	
20a	
21a	
22a	
23a	
24a	J603 M
25a	J603 L
26a	
27a	J603 P
28a	J603 N
29a	
30a	
31a	
32a	
33a	J603 I
34a	J603 I
35a	
36a	
37a	
38a	J603 W
39a	J603 Y
40a	J603 Y
41a	J603 X
42a	
43a	J606 A
44a	
45a	J649 6
50a	J616 50b, J617 50b, J617 1a

Pin No.	Connected to
1b	J617 1a, J618 1a
2b	
3b	J616 37b
4b	J615 18a
5b	J615 13a
6b	J615 19b
7b	J615 22a
8b	
9b	
10b	J617 41b
11b	
12b	
13b	J615 8b
14b	J615 2b
15b	J615 12b
16b	J615 11b
17b	J616 23b
18b	J616 33b
19b	J615 38b
20b	J615 33a
21b	J615 43a
22b	J615 44a
23b	J611 48a
24b	
25b	
26b	
27b	
28b	
29b	J615 29b
30b	J615 23b
31b	J615 30a
32b	J615 28a
33b	
34b	J611 46a
35b	J606 K
36b	J611 44a
37b	
38b	
39b	J616 22b
40b	
41b	J616 41b, J618 41b, J617 10b
42b	
43b	
44b	J616 44b, J618 44b
45b	
46b	J616 46b, J618 46b
47b	
48b	J616 48b, J618 48b
49b	
50b	J617 50a, J618 50a

(*i*) Wiring to J618.

Pin No.	Connected to	Pin No.	Connected to
1a	J617 – 1b, J618 – 1b, J618 – 50a	1b	J618 – 1a, J619 – 1a
2a		2b	
3a		3b	
4a		4b	
5a		5b	
6a		6b	
7a		7b	
8a		8b	
9a		9b	
10a		10b	J618 – 41b
11a		11b	
12a		12b	
13a		13b	
14a		14b	
15a		15b	
16a		16b	
17a		17b	
18a		18b	
19a		19b	
20a		20b	
21a		21b	
22a		22b	
23a		23b	
24a		24b	
25a		25b	
26a		26b	
27a		27b	
28a		28b	
29a		29b	
30a		30b	
31a		31b	
32a		32b	
33a		33b	
34a		34b	
35a		35b	
36a		36b	
37a		37b	
38a		38b	
39a		39b	
40a		40b	
41a		41b	J617 – 41b, J619 – 41b, J618 – 10b
42a		42b	
43a		43b	
44a		44b	J617 – 44b, J619 – 44b
45a		45b	
46a		46b	J617 – 46b, J619 – 46b
47a		47b	
48a		48b	J617 – 48b, J619 – 48b
49a		49b	
50a	J617 – 50b, J618 – 50b, J618 – 1a	50b	J618 – 50a, J619 – 50a

(7) Wiring to J619.

Pin No.	Connected to	Pin No.	Connected to
1a	J618 1b, J619 1b, J619 50a	1b	J619 1a
2a		2b	
3a		3b	
4a		4b	
5a		5b	
6a		6b	
7a		7b	
8a		8b	
9a		9b	
10a		10b	J619 41b, P621 5
11a		11b	
12a		12b	
13a		13b	
14a		14b	
15a		15b	
16a		16b	
17a		17b	
18a		18b	
19a		19b	
20a		20b	
21a		21b	
22a		22b	
23a		23b	
24a		24b	
25a		25b	
26a		26b	
27a		27b	
28a		28b	
29a		29b	
30a		30b	
31a		31b	
32a		32b	
33a		33b	
34a		34b	
35a		35b	
36a		36b	
37a		37b	
38a		38b	
39a		39b	
40a		40b	
41a		41b	J618 41b, J619 10b
42a		42b	
43a		43b	
44a		44b	J618 44b, P621 3
45a		45b	
46a		46b	J618 46b, P621 2
47a		47b	
48a		48b	J618 48b, P621 1
49a		49b	
50a	J618 50b, J619 50b, J619 1a	50b	J619 50a, P621 4

APPENDIX 5

Wiring Details for Connecting Cables and Adaptors Used with the Data Processor and Associated Data Acquisition Equipment

The cables required for the data processor and the associated data acquisition equipment are indicated in Figure 29. As indicated in Appendix 1 chassis mounted connectors are given a "J" prefix and mating cable connectors are given a "P" prefix. Mating connectors are given the same number identification. Any identification details which are marked on the various units of the data acquisition equipment are included within the various blocks of Figure 29.

For convenience, the analogue inputs to the multiplexer in the DSE Model 480001 and those to the multiplexer in the Airborne Data Processor are taken to Input Adaptor Type A units which allow up to eight inputs to be individually connected (via J11 to J18) per unit. Similarly the data processor outputs for the analogue tape recorder are taken to Output Adaptor Type A or Type B (for serial and parallel systems of digital recording respectively) from which the various data channels may be individually connected to the recording amplifier inputs. Power Adaptor Type A allows convenient connection of the 28 V (nominal) supply to up to four units via four-pin connectors J41 to J44 and also to the analogue recording equipment (Ampex Model AR200) via an eight-pin connector J45.

The various cables have been given an identification (e.g. CBL4) in Figure 29. Identical cables used for different connections have been given the same reference number.

In the following, the connector types will be first listed, then the cable and the adaptor wiring details will be given.

5.1 Connectors External to the Data Processor

Legend	Description
P11 → P18	Socket, cable, Cannon type TM-R539N-11.
J11 → J18	Plug, chassis, Cannon type TM-R575N.
J19	Socket, chassis, Cannon type KPT02-E-24-61S.
P19A → P19E	Plug, cable, Cannon type KPT06-A-24-61P with MS3057-16A cable clamp.
P501	Socket, cable, Cannon type KPT06-A-8-3S with MS3057-3A cable clamp.
P502	Socket, cable, Cannon type KPT06-A-14-19S with MS3057-8A cable clamp.
P503	Plug, cable, Cannon type KPT06-A-24-61P with MS3057-16A cable clamp.
P504	Socket, cable, Cannon type KPT06-A-24-61SW with MS3057-16A cable clamp.
P505	Socket, cable, Cannon type KPT06-A-24-61SX with MS3057-16A cable clamp.
P506	Socket, cable, Cannon type KPT06-A-24-61SY with MS3057-16A cable clamp.
P507	Socket, cable, Cannon type KPT06-A-24-61SZ with MS3057-16A cable clamp.
P601	Socket, cable, Cannon type KPT06-A-8-4S with MS3057-3A cable clamp.
P602	As for P11.
P603	Plug, cable, Cannon type KPT06-A-16-26P with MS3057-10A cable clamp.
P604, P605	As for P502.
P606	Plug, cable, Cannon type KPT06-A-14-18P with MS3057-8A cable clamp.
P607	Socket, cable, Cannon type KPT06-A-18-32SY with MS3057-12A cable clamp.
P608	Socket, cable, Cannon type KPT06-A-18-32SW with MS3057-12A cable clamp.
P609	Plug, cable, Cannon type KPT06-A-18-32PX with MS3057-12A cable clamp.
P701	Socket, cable, Cannon type KPT06-A-18-32SX with MS3057-12A cable clamp.
P26	Socket, cable, Cannon type KPT06-A-16-26SW with MS3057-10A cable clamp.
J21 → J25	Socket, chassis, BNC single hole mount jack receptacle, type [illegible]
J26	Plug, chassis, Cannon type KPT02-E-16-26PW.
P21 → P25	Plug, cable, BNC type 24931 28P102-8.
J31 → J37	As for J21.
J38	As for J26.
P31 → P37	As for P21.
J41 → J44	Socket, chassis, Cannon type KPT02-E-8-4S.
J45	Socket, chassis, Cannon type KPT02-E-16-8S.
J46	Plug, chassis, Cannon type KPT02-E-16-8P.
P41, P42	Plug, cable, Cannon type KPT06-A-8-4P with MS3057-3A cable clamp.
P45	Plug, cable, Cannon type KPT06-A-16-8P with MS3057-10A cable clamp.
P46	Socket, cable, Cannon type KPT06-A-16-8S with MS3057-10A cable clamp.
P101	As for P46.

5.2 Cable Wiring Details

The following types of individual cable are used in the various composite cables.

Legend	Description
W1	Cable, twisted pair (black and white insulation respectively) shielded, Raychem type 44A1121-22-9-0-9.
W2	Cable, twisted pair (black and white insulation respectively) shielded, Raychem type 44A1111-22-9-9.
W3	Cable, single core co-axial, 125 ohm impedance, Raychem type 44A1111-26-9-9.
W4	Cable, single core co-axial, type RG-58A/U.
W5	Cable, single core, insulated, Raychem type 44A0111-22-9.
W6	Cable, three conductors within single shield, Raychem type 44A1131-18-0 2 9-9, 18AWG effective conductor size.
W7	Cable, single conductor within shield, Raychem type 44A111-12-9-9, 12AWG effective conductor size.

Individual wires in a W1 cable are identified as W1-3 - Black, W1-3 - White and W1-3 - Shield where the "3" is an individual cable reference number (differs for each individual cable within the composite cable).

Each cable will now be considered in turn.

(*a*) CBL 1 (33 required): P11 (etc.) to open leads (to be connected to analogue transducers etc.), P602 to open leads (to be connected to speech signal output of appropriate amplifier).

Pin of P11	Signal description	Wire details
1	"Low" side of input	W2-1 - Black
2	"High" side of input	W2-1 - White
Body	Cable shield	W2-1 - Shield

(*b*) CBL 2 (1 required): P19A to P504 - Input cable for channels 1 to 8 of analogue multiplexer (part of DSE Model 480001).

Interconnections		Signal description	Wire details
Pin of P19A	Pin of P504		
A			
B	B	Input 0 shield	W1-1 - Shield
C			
D			
E			
F	F	Input 1 shield	W1-2 - Shield
G			
H			
J			
K	K	Input 2 shield	W1-3 - Shield
L			

Interconnections		Signal description	Wire details
Pin of P19A	Pin of P504		
M			
N			
P	P	Input 3 shield	W1-4—Shield
R			
S			
T			
U	U	Input 4 shield	W1-5—Shield
V			
W			
X			
Y	Y	Input 5 shield	W1-6—Shield
Z	Z	Input adaptor type A case ground	W5
a			
b			
c	c	Input 0 high	W1-1—White
d	d	Input 0 low	W1-1—Black
e			
f	f	Input 1 high	W1-2—White
g	g	Input 1 low	W1-2—Black
h			
i	i	Input 2 high	W1-3—White
j	j	Input 2 low	W1-3—Black
k			
m	m	Input 3 high	W1-4—White
n	n	Input 3 low	W1-4—Black
p			
q	q	Input 4 high	W1-5—White
r	r	Input 4 low	W1-5—Black
s			
t	t	Input 5 high	W1-6—White
u	u	Input 5 low	W1-6—Black
v			
w			
x			
y			
z			
AA			
BB			
CC			
DD			
EE			
FF			
GG			
HH	HH	Input 6 shield	W1-7—Shield
JJ	JJ	Input 6 high	W1-7—White
KK	KK	Input 7 high	W1-8—White
LL	LL	Input 7 shield	W1-8—Shield
MM	MM	Input 7 low	W1-8—Black
NN	NN	Input 6 low	W1-7—Black
PP			

(*c*) CBL 3, CBL 4 and CBL 5A (1 of each required): P19B to P505, P19C to P506, and P19D to P507 Input cables for channels 9 to 32 of analogue multiplexer.

Connections are identical to those indicated for CBL 2 but the cables are not interchangeable (at the multiplexer ends) as the inserts in the connectors are rotated relative to each other.

(*d*) CBL 5 (1 required): P19E to P607 Input cable for analogue signals to be multiplexed in the data processor.

Interconnections		Signal description	Wire details
Pin of P19E	Pin of P607		
A			
B	A	Input 0 shield	W1-1 Shield
C			
D			
E			
F	C	Input 1 shield	W1-2 Shield
G			
H			
J			
K	E	Input 2 shield	W1-3 Shield
L			
M			
N			
P	G	Input 3 shield	W1-4 Shield
R			
S			
T			
U	J	Input 4 shield	W1-5 Shield
V			
W			
X			
Y	L	Input 5 shield	W1-6 Shield
Z	S	Input adaptor type A case ground	W5
a			
b			
c	T	Input 0 high	W1-1 White
d	U	Input 0 low	W1-1 Black
e			
f	B	Input 1 high	W1-2 White
g	V	Input 1 low	W1-2 Black
h			
i	D	Input 2 high	W1-3 White
j	W	Input 2 low	W1-3 Black
k			
m	F	Input 3 high	W1-4 White
n	Y	Input 3 low	W1-4 Black
p			
q	H	Input 4 high	W1-5 White
r	Z	Input 4 low	W1-5 Black
s			

Interconnections		Signal description	Wire details
Pin of P19E	Pin of P607		
t	K	Input 5 high	W1-6—White
u	a	Input 5 low	W1-6—Black
v			
w			
x			
y			
z			
AA			
BB			
CC			
DD			
EE			
FF			
GG			
HH	N	Input 6 shield	W1-7—Shield
JJ	M	Input 6 high	W1-7—White
KK	P	Input 7 high	W1-8—White
LL	R	Input 7 shield	W1-8—Shield
MM	d	Input 7 low	W1-8—Black
NN	c	Input 6 low	W1-7—Black
PP			

(*e*) CBL 6A and CBL 6B: P501 to P42, P601 to P41—Input power cables for multiplexer, ADC and for data processor.

CBL 6A DETAILS

Interconnection		Signal description	Wire details
Pin of P501	Pin of P42		
A	A	+28 V	W6—Red
B	B	28 V return	W6—Black
C	C, D*	Case ground, cable shield	W6—Brown, W6—Shield

* Jumper brown lead and shield *only* at the P501 end.

CBL 6B DETAILS

Interconnection		Signal description	Wire details
Pin of P601	Pin of P41		
A	A	+28 V	W6—Red
B	B	28 V return	W6—Black
C	C	Case ground	W6—Brown
D	D	Cable shield	W6—Shield

(f) CBL 7 (1 required): P502 to P606 Inputs of multiplexer/ADC from data processor.

Interconnections		Signal description	Wire details
Pin of P502	Pin of P606		
A	A	Command to convert	W3-1 Inner
B	B	Random/sequential control	W3-2 Inner
C	C	Auto/programmed range control	W3-3 Inner
D	D	Gain range control 1	W3-4 Inner
E	E	Gain range control 2	W3-5 Inner
F	F	Gain range control 4	W3-6 Inner
G	G	Gain range control 8	W3-7 Inner
H	H	Digital common	Shields W3-4 to W3-7
J	J	+5 V (to spare pin on ADC)	W3-8 Inner
K	K	System reset	W3-9 Inner
L	L	Multiplexer control 1	W3-10 Inner
M	M	Multiplexer control 2	W3-11 Inner
N	N	Multiplexer control 4	W3-12 Inner
P	P	Multiplexer control 8	W3-13 Inner
R	R	Multiplexer control 16	W3-14 Inner
S	S	Digital common	Shield W3-10 to W3-14
T	T	Digital common	Shields W3-1 to W3-3, W3-8 and W3-9
U	U	Multiplexer/ADC chassis	W5
V			

(g) CBL 8 (1 required): P503 to P608 - Inputs to data processor from multiplexer ADC.

Interconnections		Signal description	Wire details
Pin of P503	Pin of P608		
A	D	ADC Bit 4 (sign)	W3-1 Inner
B	E	ADC Bit 5 (MSB)	W3-2 Inner
C	X	ADC Bit 6	W3-3 Inner
D	Y	ADC Bit 7	W3-4 Inner
E	G	ADC Bit 8	W3-5 Inner
F	H	ADC Bit 9	W3-6 Inner
G	Z	ADC Bit 10	W3-7 Inner
H	a	ADC Bit 11	W3-8 Inner
J	L	ADC Bit 12	W3-9 Inner
K	M	ADC Bit 13	W3-10 Inner
L	b	ADC Bit 14	W3-11 Inner
M	c	ADC Bit 15 (LSB)	W3-12 Inner
N	P	CLK (unused output from data processor)	W3-13 Inner

Interconnections		Signal description	Wire details
Pin of P503	Pin of P608		
P	F	Digital common	Shields W3-1 to W3-4
R	V	ADC Bit 3 (Range "1")	W3-14—Inner
S	U	ADC Bit 2 (Range "2")	W3-15—Inner
T			
U			
V	C	Digital common	Shields W3-14 to W3-17
W			
X			
Y			
Z			
a			
b	J	Digital common	Shields W3-5 to W3-8
c	T	Multiplexer/ADC chassis	W5
d	R	GATE (unused output from data processor)	W3-18—Inner
e	d		W3-19—Inner
f	e	Over-range	W3-20—Inner
g			
h			
i			
j			
k			
m			
n			
p			
q			
r			
s			
t			
u			
v			
w	N	Digital common	Shields W3-9 to W3-12
x			
y			
z	B	ADC Bit 1 (Range "4")	W3-16—Inner
AA	A	ADC Bit 0 (Range "8")	W3-17—Inner
BB	S	Digital common	Shields W3-13, W3-18 to W3-20
CC			
DD			
EE			
FF			
GG			
HH			
JJ			
KK			
LL			
MM			
NN			
PP			

(*h*) CBL 9 (2 required): P604 and P605 to open ends (to be connected to outputs of digital transducers).

Pin of P604, P605	Signal description	Wire details
A	Bit 0 (most significant bit)	W3-1 Inner
B	Bit 1	W3-2 Inner
C	Bit 2	W3-3 Inner
D	Bit 3	W3-4 Inner
E	Bit 4	W3-5 Inner
F	Bit 5	W3-6 Inner
G	Bit 6	W3-7 Inner
H	Bit 7	W3-8 Inner
J	Bit 8	W3-9 Inner
K	Bit 9	W3-10 Inner
L	Bit 10	W3-11 Inner
M	Digital common	Shields W3-1 to W3-18
N	Spare	W3-12 Inner
P	Bit 11	W3-13 Inner
R	Bit 12	W3-14 Inner
S	Bit 13	W3-15 Inner
T	Bit 14	W3-16 Inner
U	Spare	W3-17 Inner
V	Bit 15	W3-18 Inner

(*i*) CBL 10 (1 required): P609 to P701 Time-of-day display output of data processor (PDM clock also taken out here).

Interconnections		Signal description	Wire details
Pin of P609	Pin of P701		
A	A	1-line seconds, units	W3-1—Inner
B	B	2-line seconds, units	W3-2—Inner
C	C	4-line seconds, units	W3-3—Inner
D	D	8-line seconds, units	W3-4—Inner
E	E	1-line seconds, tens	W3-5—Inner
F	F	2-line seconds, tens	W3-6—Inner
G	G	4-line seconds, tens	W3-7—Inner
H	H	1-line minutes, units	W3-8—Inner
J	J	2-line minutes, units	W3-9—Inner
K	K	4-line minutes, units	W3-10—Inner
L	L	8-line minutes, units	W3-11—Inner
M	M	1-line minutes, tens	W3-12—Inner
N	N	2-line minutes, tens	W3-13—Inner
P	P	4-line minutes, tens	W3-14—Inner
R	R	1-line hours, units	W3-15—Inner
S	S	2-line hours, units	W3-16—Inner
T	T	4-line hours, units	W3-17—Inner
U	U	8-line hours, units	W3-18—Inner
V	V	1-line hours, tens	W3-19—Inner
W	W	2-line hours, tens	W3-20—Inner
X	X	28 V return	W6—Red
Y	Y	28 V (nominal) input	W6—Black
Z	Z	Time display case ground	W6—Brown
a	a	Shield	W6—Shield
b	b	Common	Shields W3-1 to W3-4
c	c	Common	Shields W3-5 to W3-7
d	d	Common	Sheilds W3-8 to W3-11
e	e	Common	Shields W3-12 to W3-14
f	f	Common	Shields W3-15 to W3-18
g	g	Common	Shields W3-19 & W3-20
h	h	PDM clock	W3-21—Inner
j	j	Common for PDM clock	W3-21—Shield

(*j*) CBL 11 (1 required): P603 to P26 Tape recorder outputs of data processor (for output adaptor type A or type B).

Interconnections		Signal description	Wire details
Pin of P603	Pin of P26		
A	A	DIR output	W3-1 Inner
B	B	Common	W3-1 Shield
C	C	FM output	W3-2 Inner
D	D	Common	W3-2 Shield
E	E	RZ output	W3-3 Inner
F	F	Common	W3-3 Shield
G	G	NRZ 1 output	W3-4 Inner
H	H	Common	W3-4 Shield
J	J	NRZ 2 output	W3-5 Inner
K	K	Common	W3-5 Shield
L	L	NRZ 3 output	W3-6 Inner
M	M	Common	W3-6 Shield
N	N	NRZ 4 output	W3-7 Inner
P	P	Common	W3-7 Shield
R	R	Adaptor case	W5
S	S		W5
T	T	NRZ 5 output	W3-8 inner
U	U	Common	W3-8 Shield
V	V	NRZ 6 output	W3-9 Inner
W	W	Common	W3-9 Shield
X	X	NRZ 7 output	W3-10 Inner
Y	Y	Common	W3-10 Shield
Z	Z		W3-11 Inner
a	a		W3-11 Shield
b	b		W3-12 Inner
c	c		W3-12 Shield

(*k*) CBL 12 (1 required): P46 to open ends (to be connected to aircraft or other supply).

Pin of P46	Signal description	Wire details
A	+ 28 V	W7-1
B	28 V return	W7-2
C		
D	28 V return	W7-3
E	+ 28 V	W7-4
F		
G	Cable shield	Shields W7-1 to W7-4
H	28 V return	Short to Pin B of P46

(*l*) CBL 13 (1 required): P45 to P101 Power input to Ampex Model AR200 analogue tape recorder.

Interconnections		Signal description	Wire details
Pin of P45	Pin of P101		
A	A	+ 28 V for transport	W7-1
B	B	28 V return	W7-2
C			
D	D	28 V return	W7-3
E	E	+ 28 V for heaters	W7-4
F			
G	G	Cable shield	Shields W7-1 to W7-4
H	H	28 V return	Short to Pin B of P45

(*m*) CBL 14 (7 required): Inputs to analogue tape recording amplifiers. Connectors as for P21 are used at each end; cable W4 is used.

5.3 Adaptor Wiring Details

(*a*) Input adaptor type A.

Input adaptor type A is wired according to the following table. The body of the input plugs J11 to J18 are insulated from the adaptor case.

Interconnections		Signal description	Wire details
Pin of J11 to J18	Pin of J19		
J11-2	c	Input 0 high	W1-1 White
J11-1	d	Input 0 low	W1-1 Black
J11—Body	B	Input 0 shield	W1-1 Shield
J12-2	f	Input 1 high	W1-2 White
J12-1	g	Input 1 low	W1-2 Black
J12—Body	F	Input 1 shield	W1-2 Shield
J13-2	i	Input 2 high	W1-3 White
J13-1	j	Input 2 low	W1-3 Black
J13—Body	K	Input 2 shield	W1-3 Shield
J14-2	m	Input 3 high	W1-4 White
J14-1	n	Input 3 low	W1-4 Black
J14—Body	P	Input 3 shield	W1-4 Shield
J15-2	q	Input 4 high	W1-5 White
J15-1	r	Input 4 low	W1-5 Black
J15—Body	U	Input 4 shield	W1-5 Shield
J16-2	t	Input 5 high	W1-6 White
J16-1	u	Input 5 low	W1-6 Black
J16—Body	Y	Input 5 shield	W1-6 Shield
J17-2	JJ	Input 6 high	W1-7 White
J17-1	NN	Input 6 low	W1-7 Black
J17—Body	HH	Input 6 shield	W1-7 Shield
J18-2	KK	Input 7 high	W1-8 White
J18-1	MM	Input 7 low	W1-8 Black
J18—Body	LL	Input 7 shield	W1-8 Shield
	Z	Adaptor case	W5

(*b*) Output adaptor type A.

Output adaptor type A is wired according to the following table. The body of each of the output (BNC) sockets is insulated from the adaptor case.

Interconnections		Signal description	Wire details
Pin of J21 to J25	Pin of J26		
J21 Inner	G	NRZ 1 output	W3-1—Inner
J21 Body	H	Common	W3-1—Shield
J22 Inner	J	NRZ 2 output	W3-2—Inner
J22 Body	K	Common	W3-2—Shield
J23 Inner	E	RZ output	W3-3—Inner
J23 Body	F	Common	W3-3—Shield
J24 Inner	A	DIR output	W3-4—Inner
J24 Body	B	Common	W3-4—Shield
J25—Inner	C	FM output	W3-5—Inner
J25—Body	D	Common	W3-5—Shield
	R	Adaptor case	W5

(*c*) Out adaptor type B.

Out adaptor type B is wired according to the following table. The body of each of the output (BNC) sockets is insulated from the adaptor case.

Interconnection		Signal description	Wire details
Pin of J31 to J37	Pin of J38		
J31 Inner	G	NRZ 1 output	W3-1—Inner
J31 Body	H	Common	W3-1—Shield
J32 Inner	J	NRZ 2 output	W3-2—Inner
J32 Body	K	Common	W3-2—Shield
J33 Inner	L	NRZ 3 output	W3-3—Inner
J33 Body	M	Common	W3-3—Shield
J34 Inner	N	NRZ 4 output	W3-4—Inner
J34 Body	P	Common	W3-4—Shield
J35 Inner	T	NRZ 5 output	W3-5—Inner
J35 Body	U	Common	W3-5—Shield
J36 Inner	V	NRZ 6 output	W3-6—Inner
J36 Body	W	Common	W3-6—Shield
J37 Inner	X	NRZ 7 output	W3-7—Inner
J37 Body	Y	Common	W3-7—Shield
	R	Adaptor case	W5

(*d*) Power adaptor type A.

Power adaptor type A is wired according to the following table.

Interconnection		Signal description	Wire details
Pin of J46	Pins of J41 to J46		
A	J41-A, J42-A, J43-A, J44-A, J45-A	+28 V	W6—red wires without shield W7 wire without shield
B	J41-B, J42-B, J43-B, J44-B, J45-B	28 V return	W6—black wires without shield W7 wire without shield
D	J45-D	28 V return for Ampex	W7 wire without shield
E	J45-E	28 V for Ampex heaters	W7 wire without shield
H	J45-H	28 V return for Ampex	

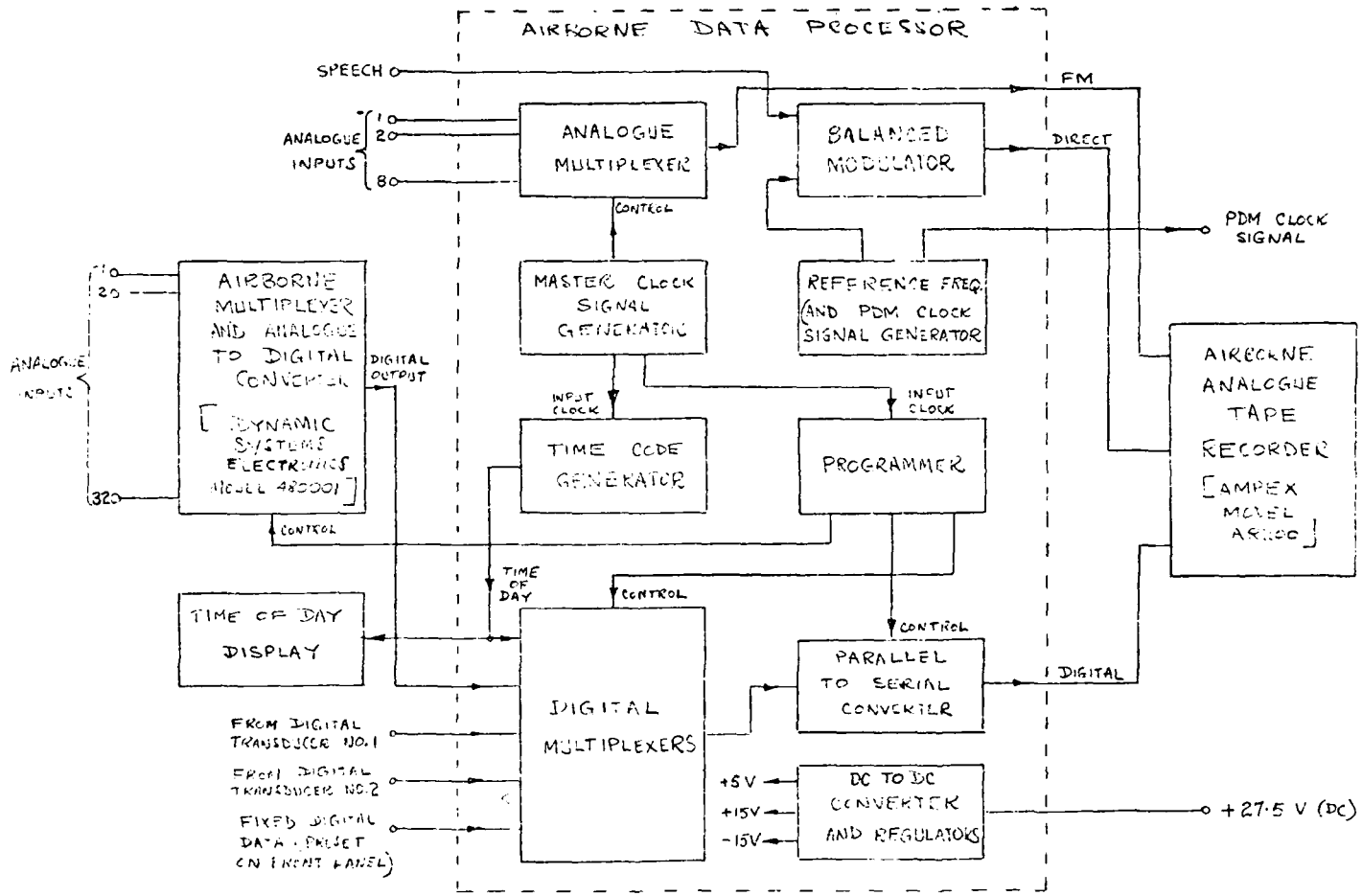


FIG. 1. BLOCK SCHEMA OF AIRBORNE DATA PROCESSOR AND ASSOCIATED EQUIPMENT

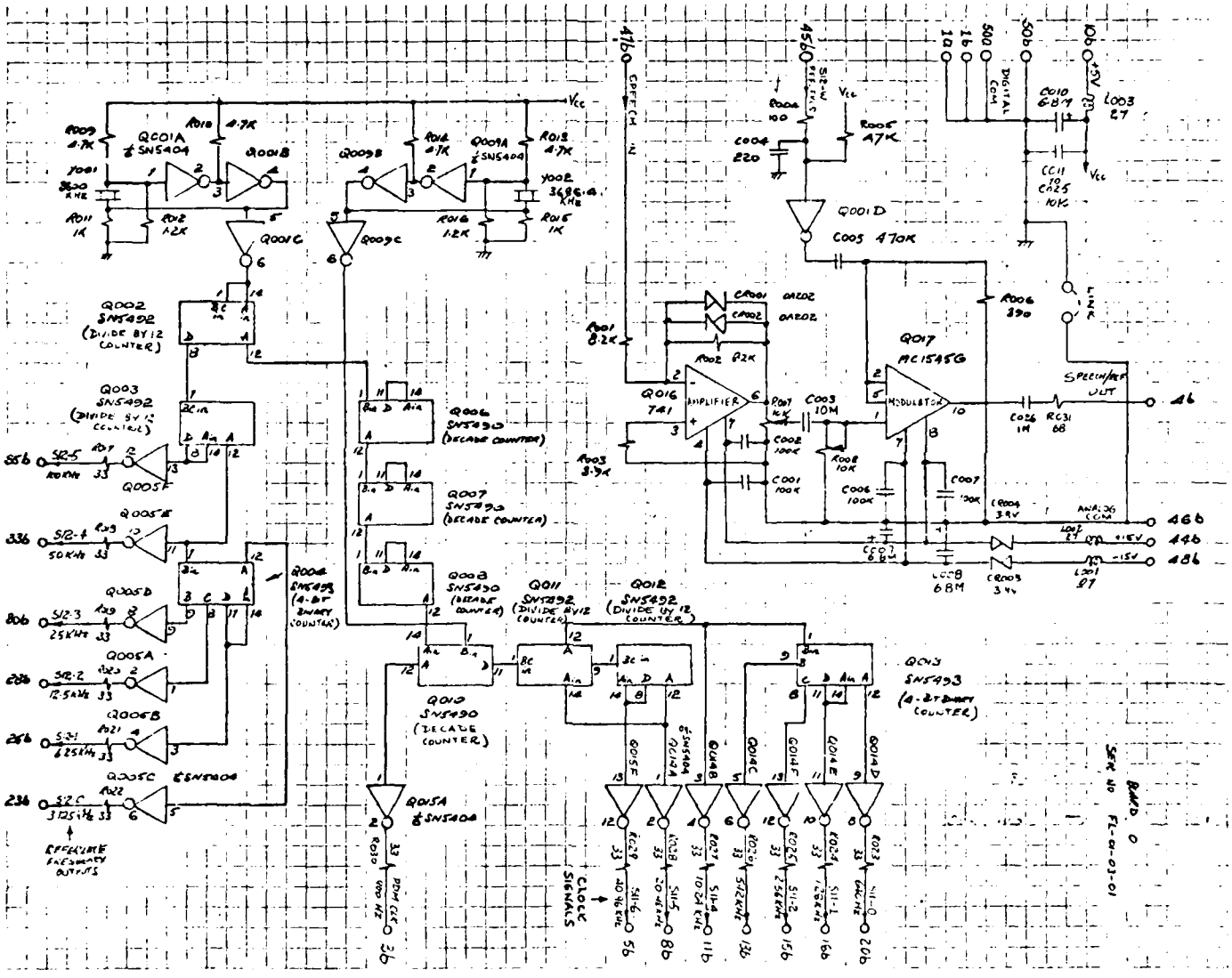


FIG. 2. TIMING SIGNALS GENERATOR AND MODULATOR

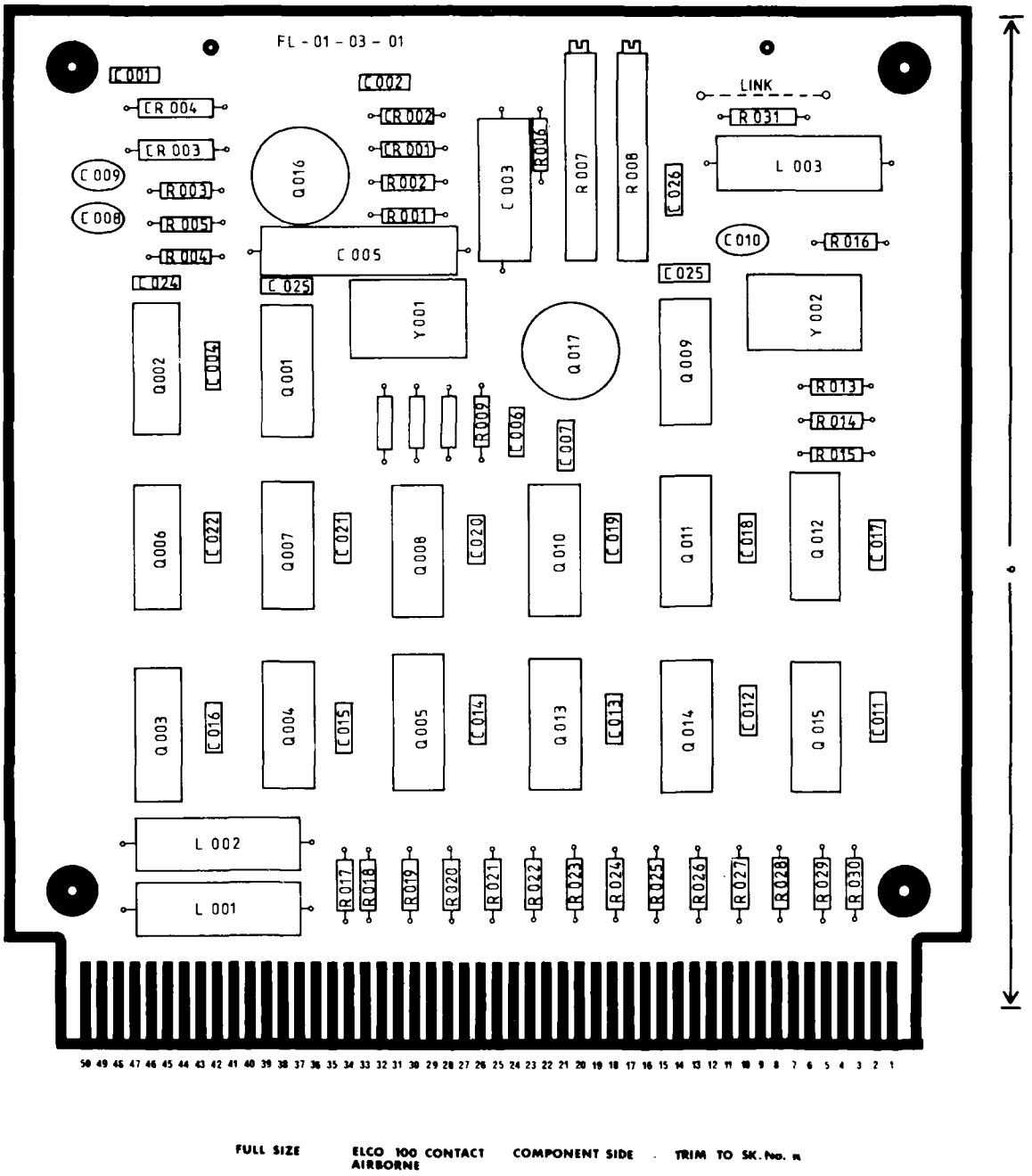


FIG. 3. COMPONENT LAYOUT FOR TIMING SIGNALS GENERATOR AND MODULATOR

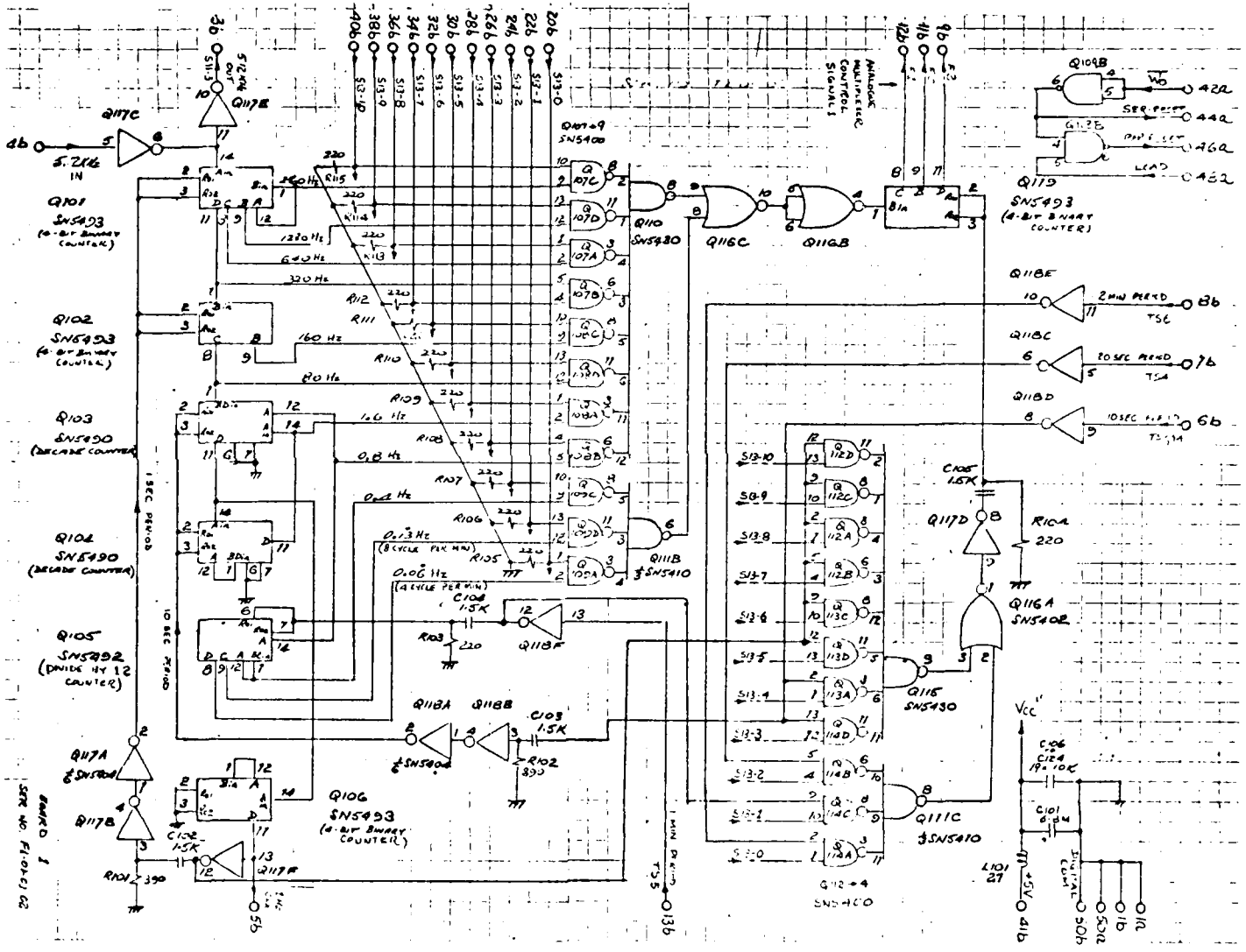


FIG. 4. ANALOGUE MULTIPLEXER CONTROL SIGNAL GENERATOR

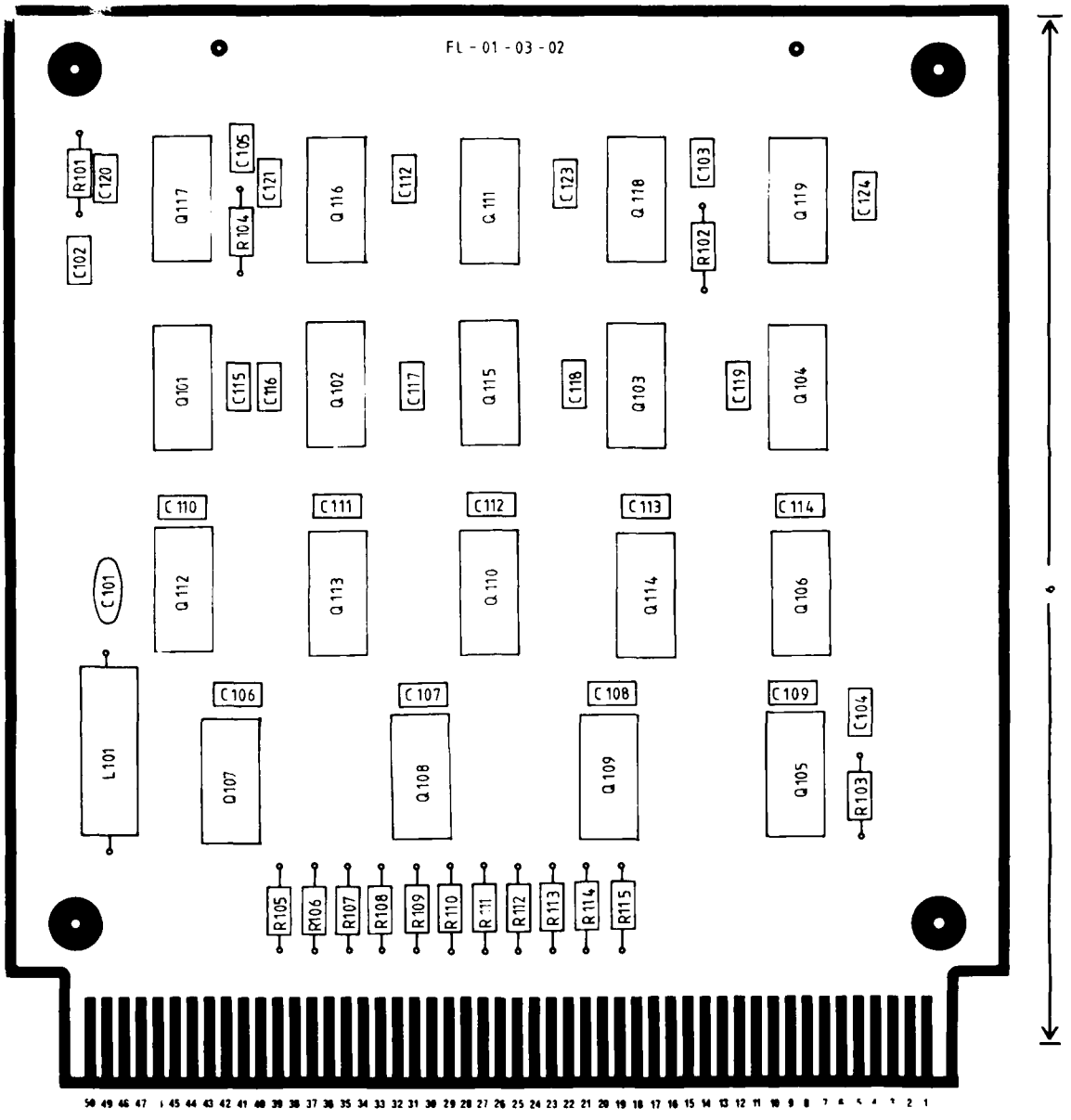


FIG. 5. COMPONENT LAYOUT FOR ANALOGUE MULTIPLEXER CONTROL SIGNAL GENERATOR

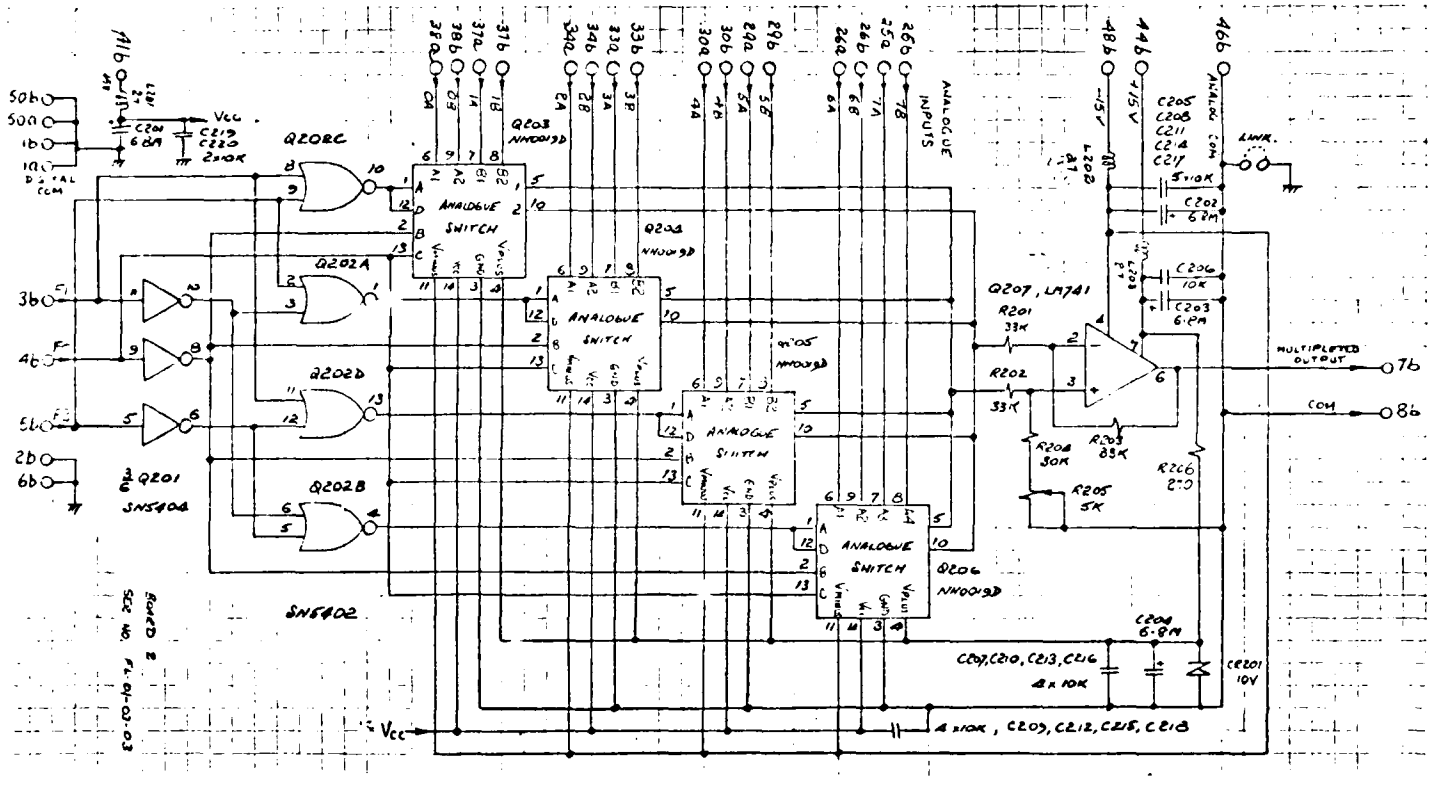


FIG. 6. ANALOGUE MULTIPLEXER

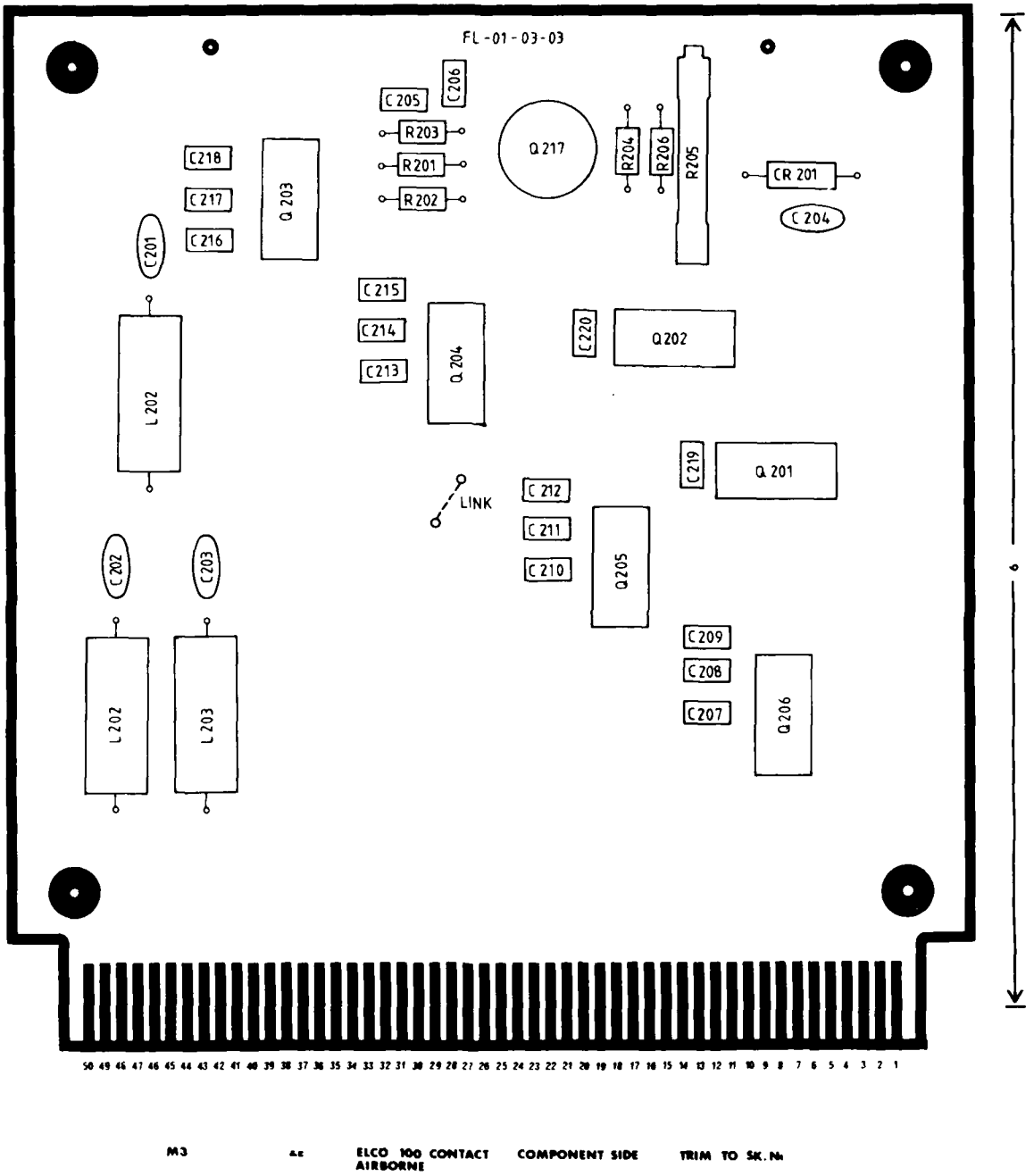


FIG. 7. COMPONENT LAYOUT FOR ANALOGUE MULTIPLEXER

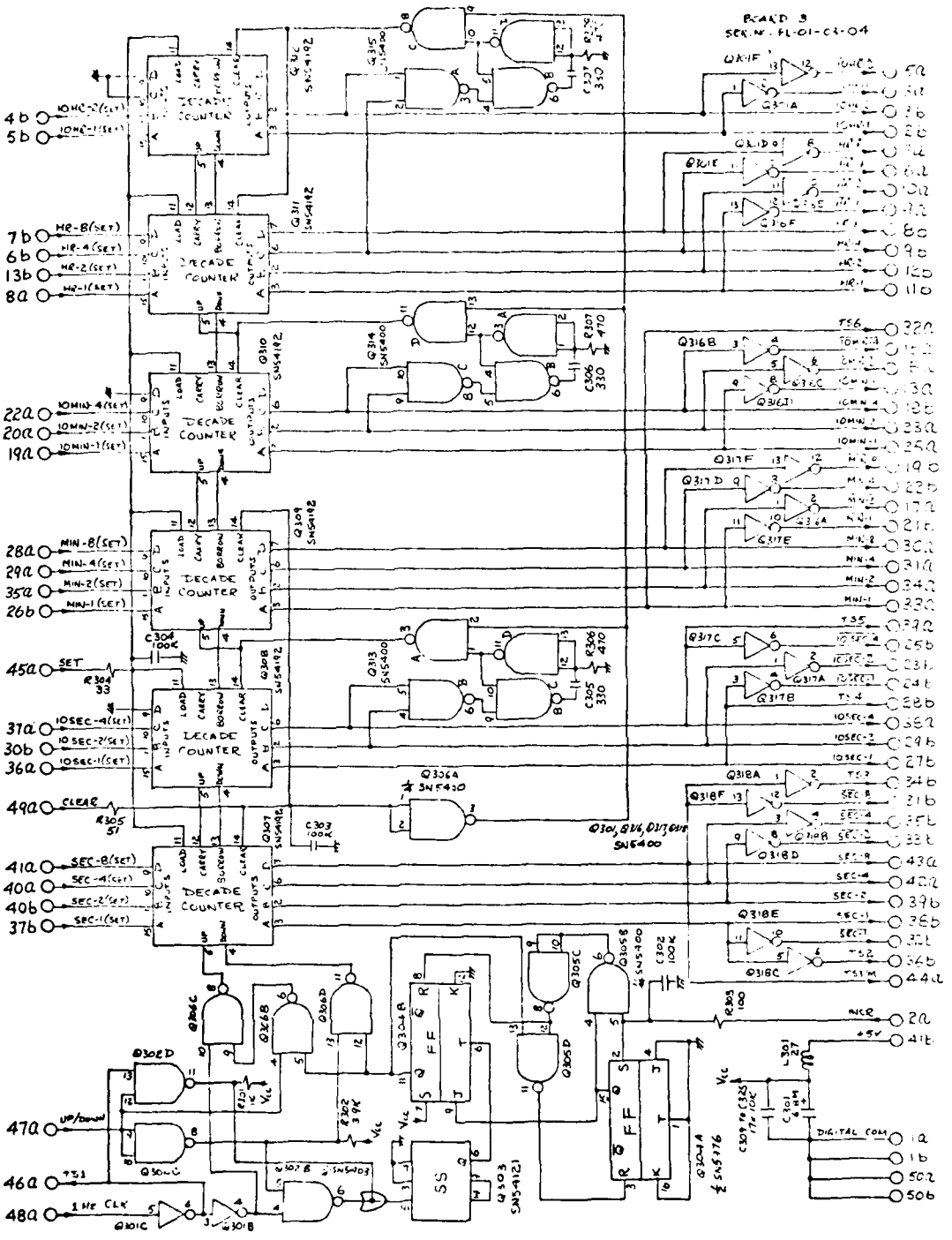


FIG. 8. TIME CODE GENERATOR

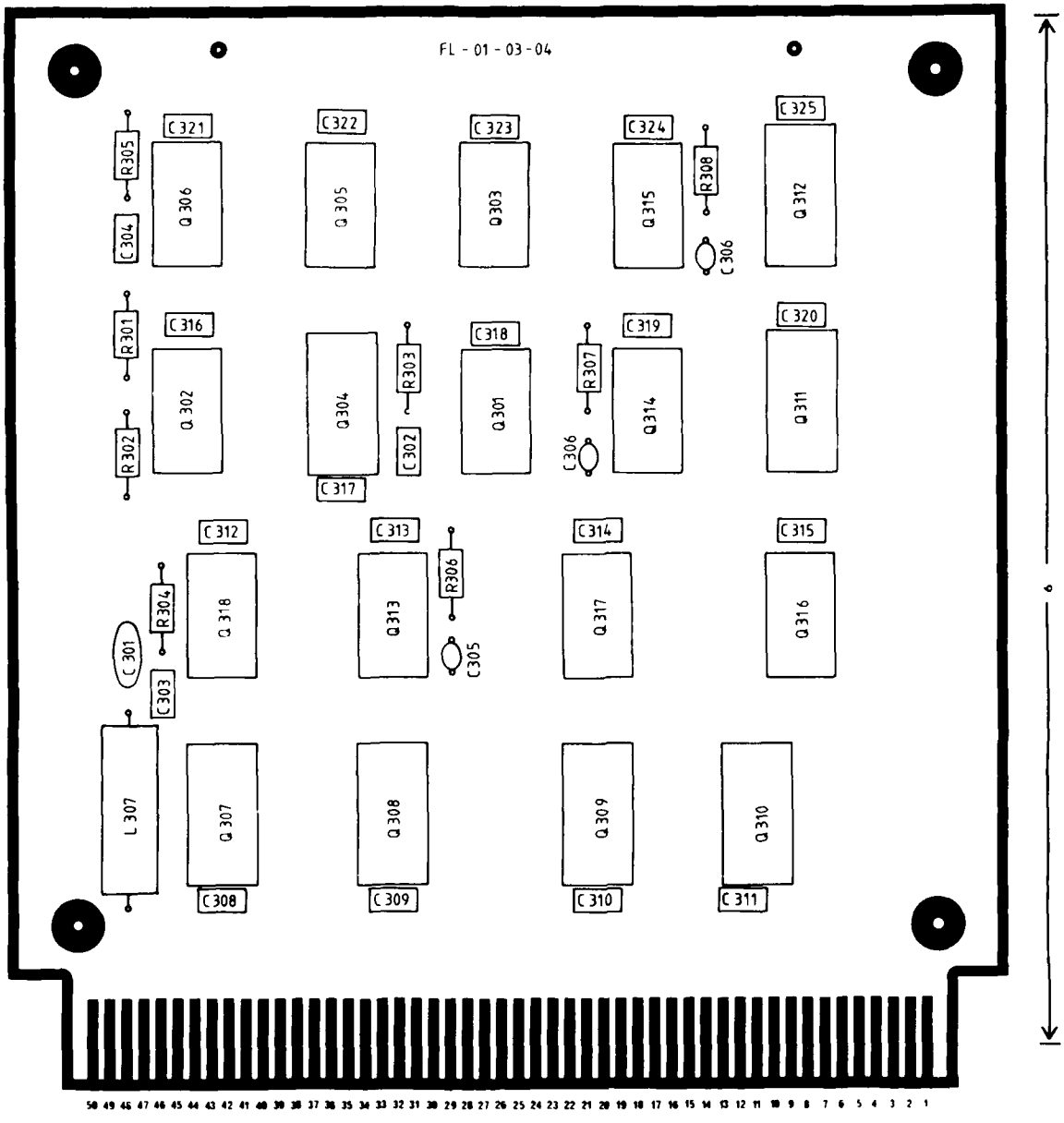


FIG. 9. COMPONENT LAYOUT FOR TIME CODE GENERATOR

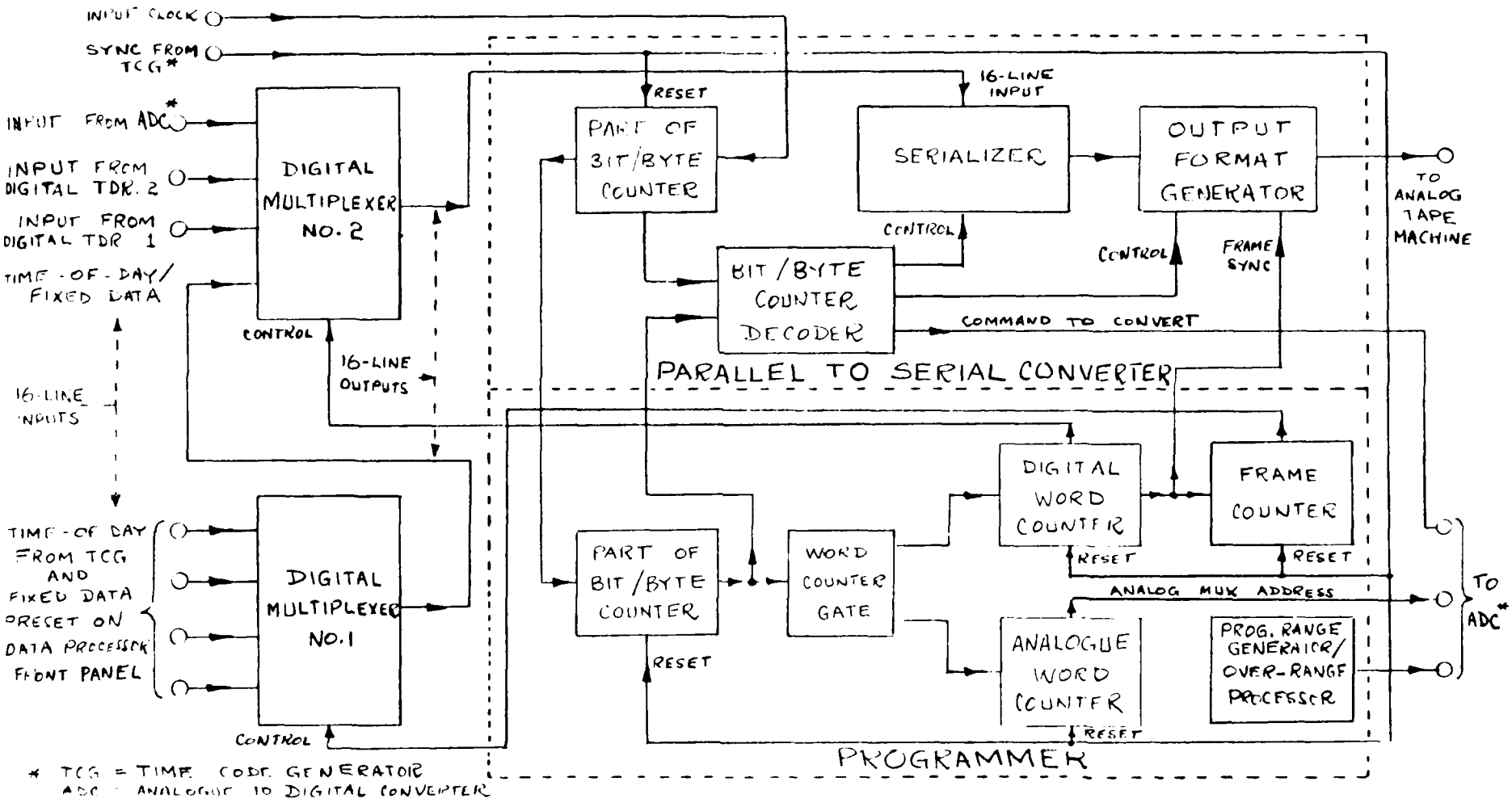


FIG. 10. BLOCK SCHEMA OF PROCESSING CIRCUITS WITH DIGITAL OUTPUTS FOR TAPE MACHINE

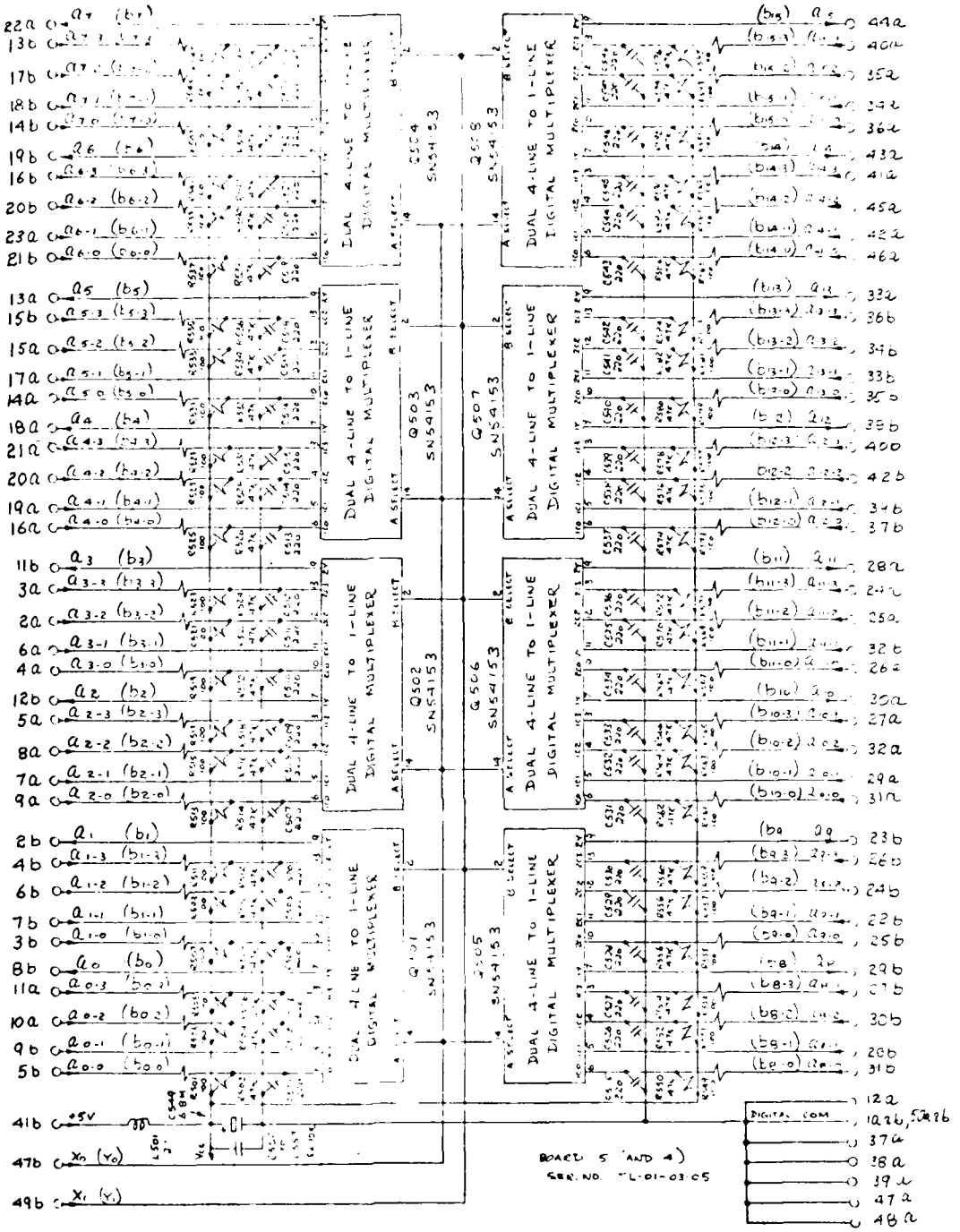
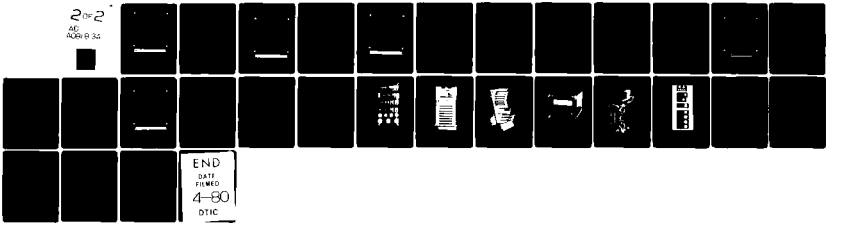
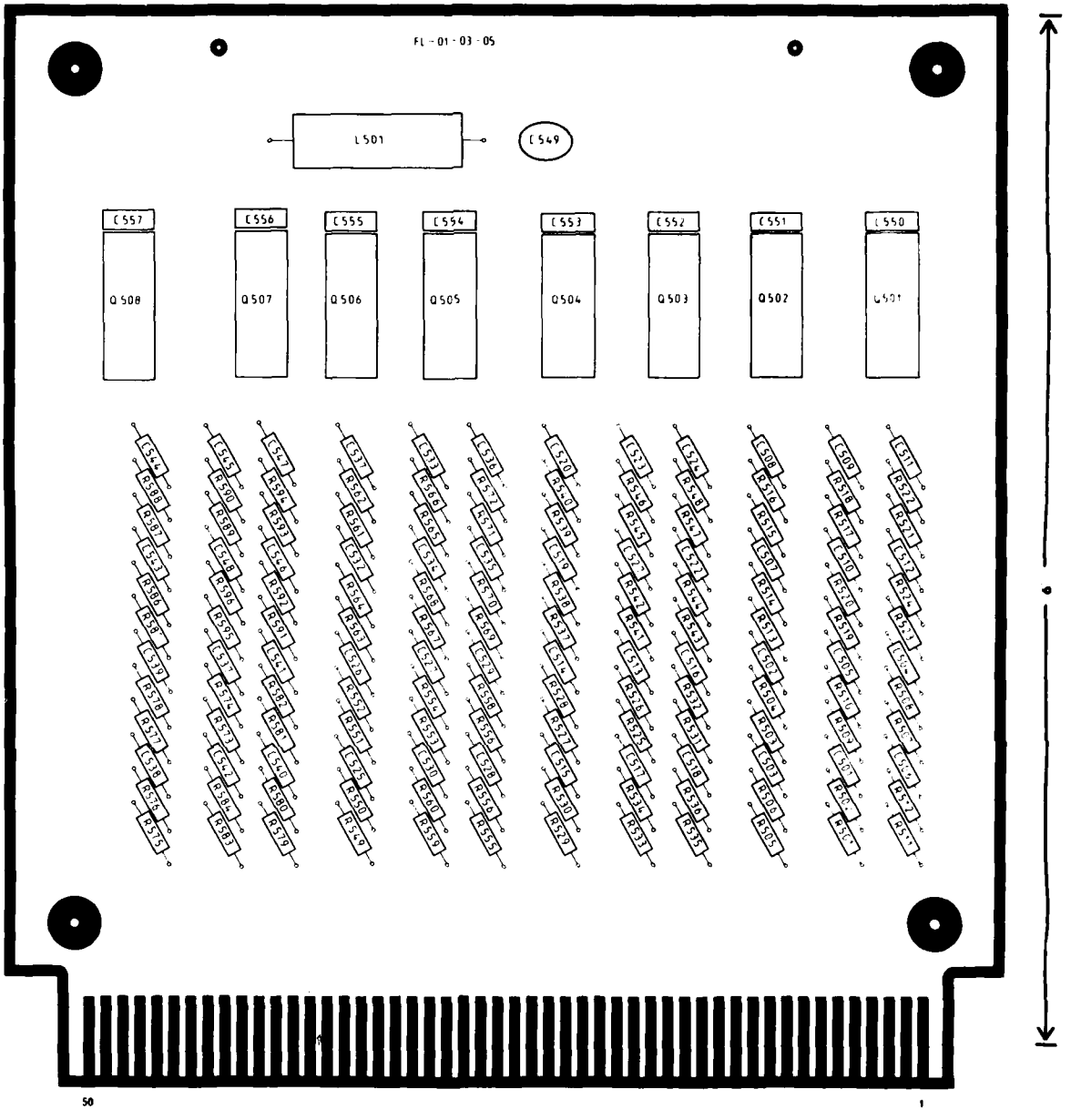


FIG. 11. DIGITAL MULTIPLEXER

AD-A081 834 AERONAUTICAL RESEARCH LABS MELBOURNE (AUSTRALIA) F/G 9/2
AIRBORNE DATA PROCESSOR.(U)
NOV 78 K F FRASER, U R KRIESER
UNCLASSIFIED ARL-MER-153 NL





M3 4 x FULL SIZE ELCO 100 CONTACT AIRBORNE COMPONENT SIDE TRIM TO SK. No. 16274

FIG. 12. COMPONENT LAYOUT FOR DIGITAL MULTIPLEXER

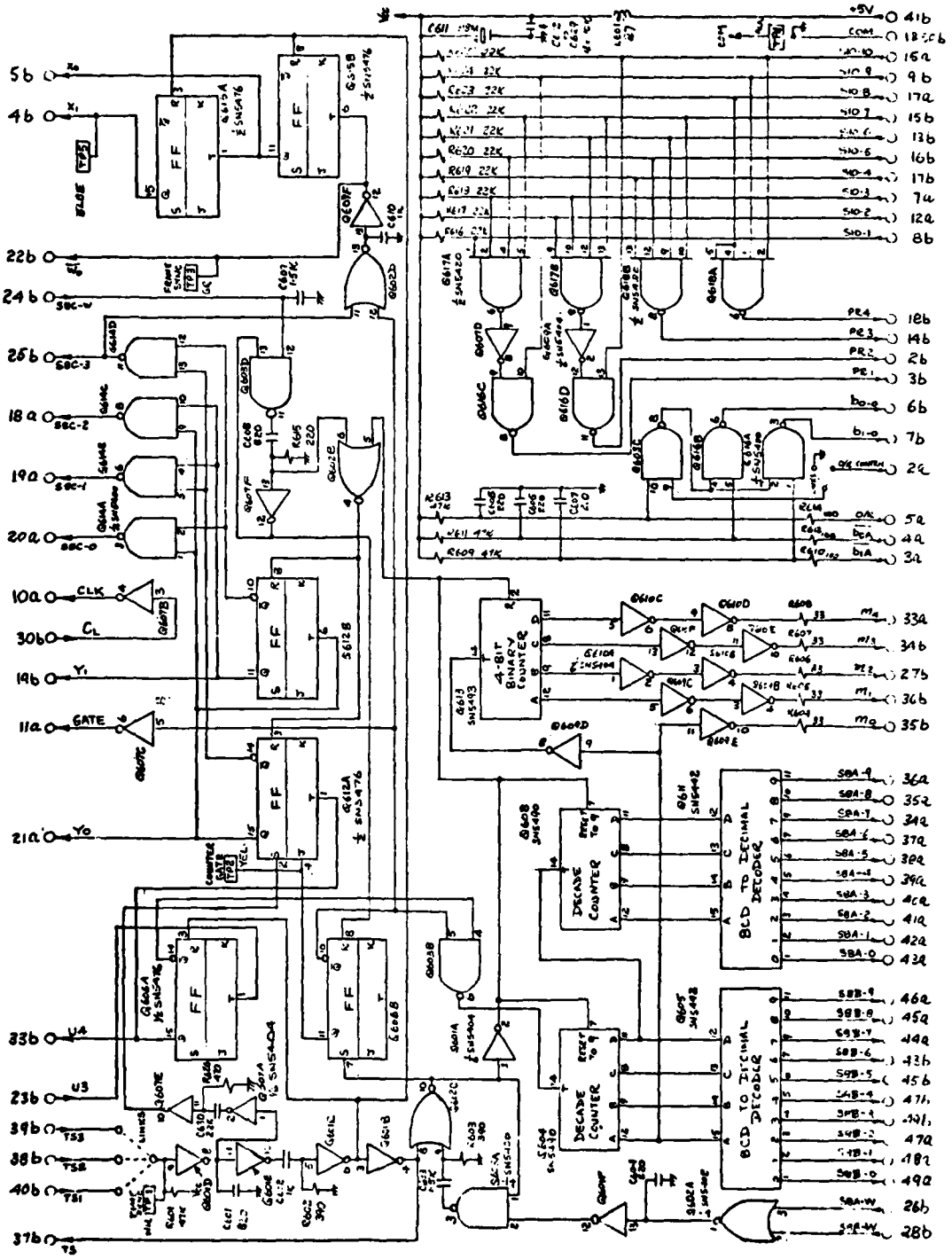


FIG. 13. PROGRAMMER

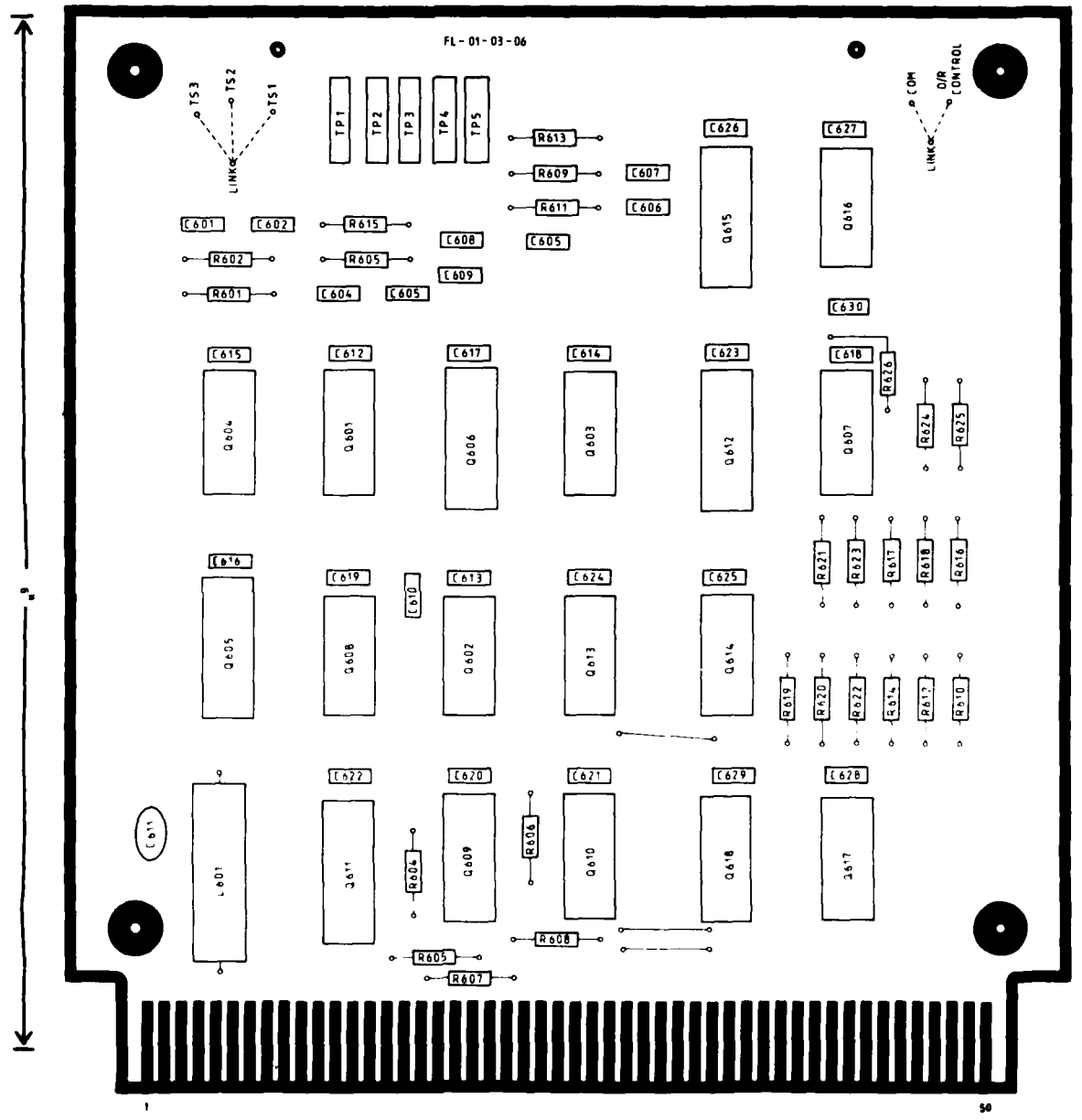


FIG. 14. COMPONENT LAYOUT FOR PROGRAMMER

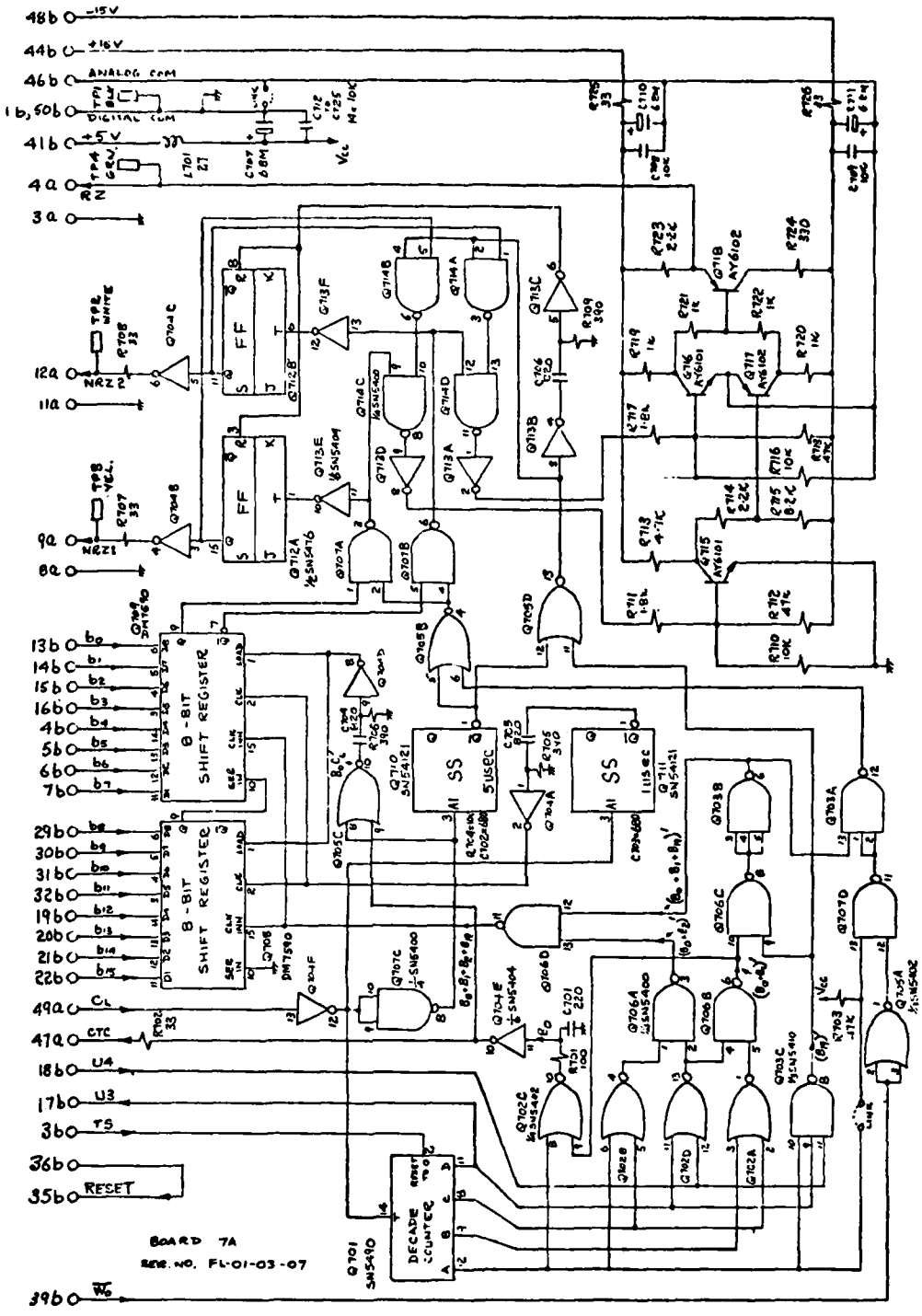


FIG. 15. PARALLEL TO SERIAL CONVERTER
(serial system)

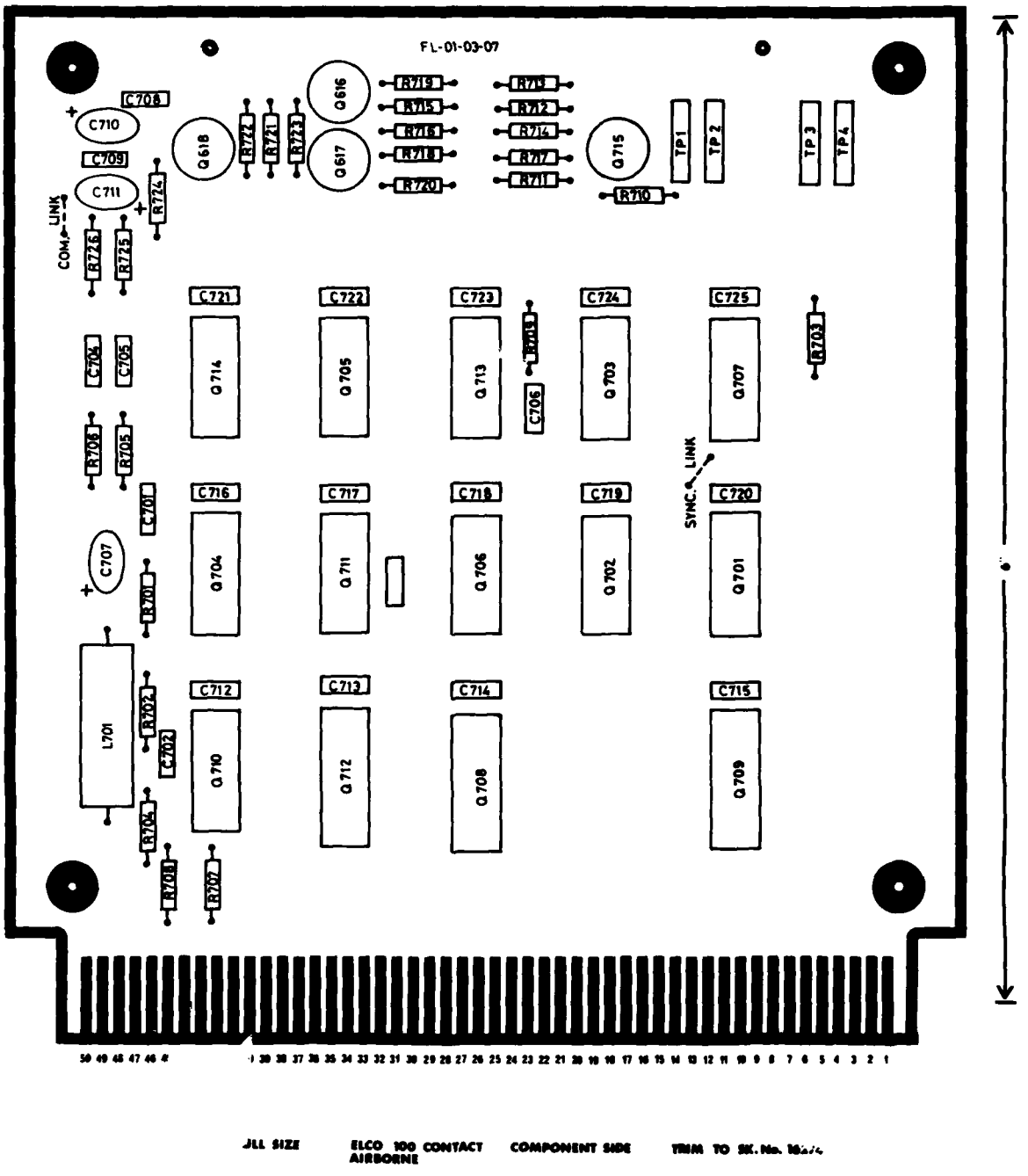


FIG. 16. COMPONENT LAYOUT FOR PARALLEL TO SERIAL CONVERTER
(serial system)

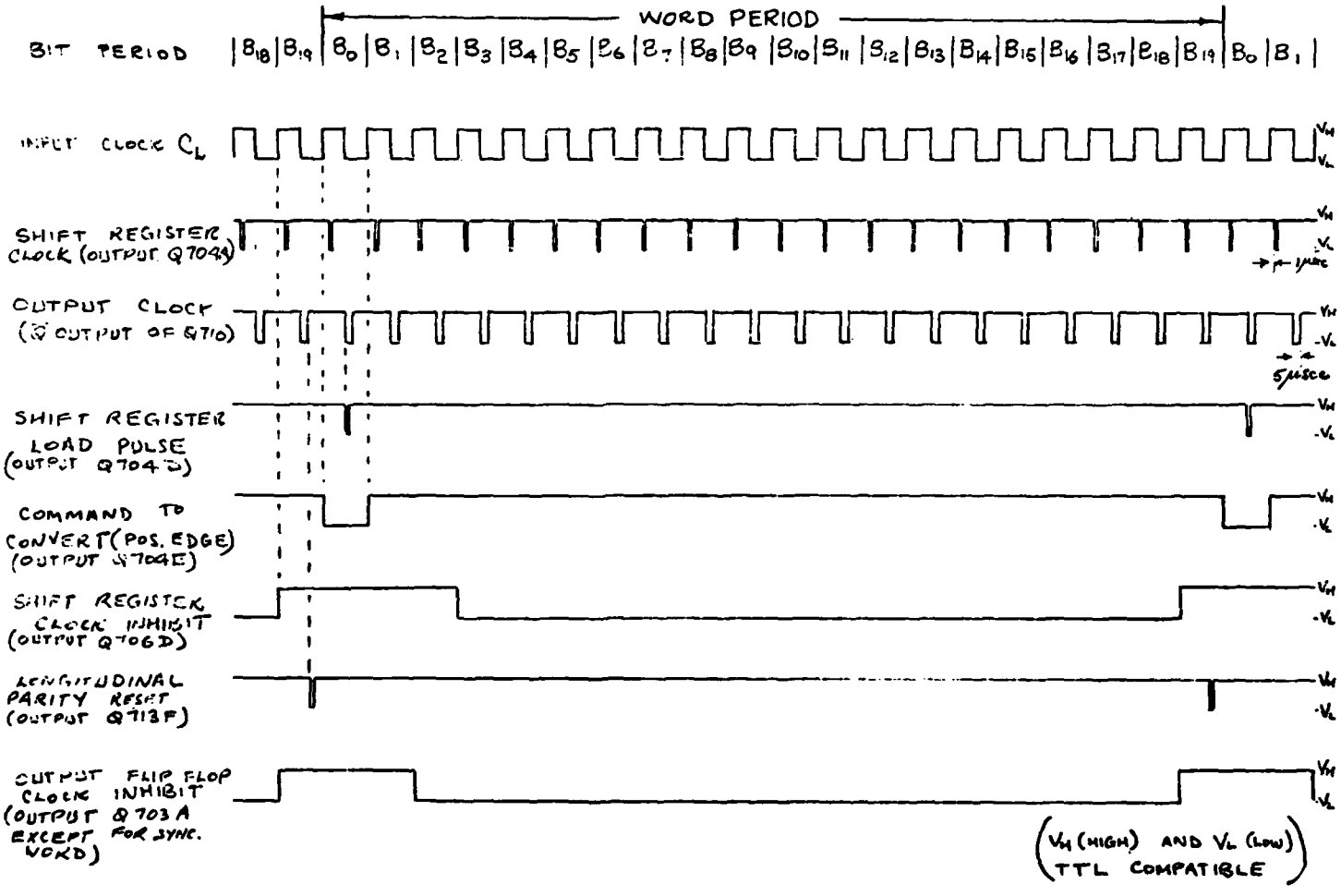


FIG. 17. CONTROL SIGNALS FOR PARALLEL TO SERIAL CONVERTER
(serial system)

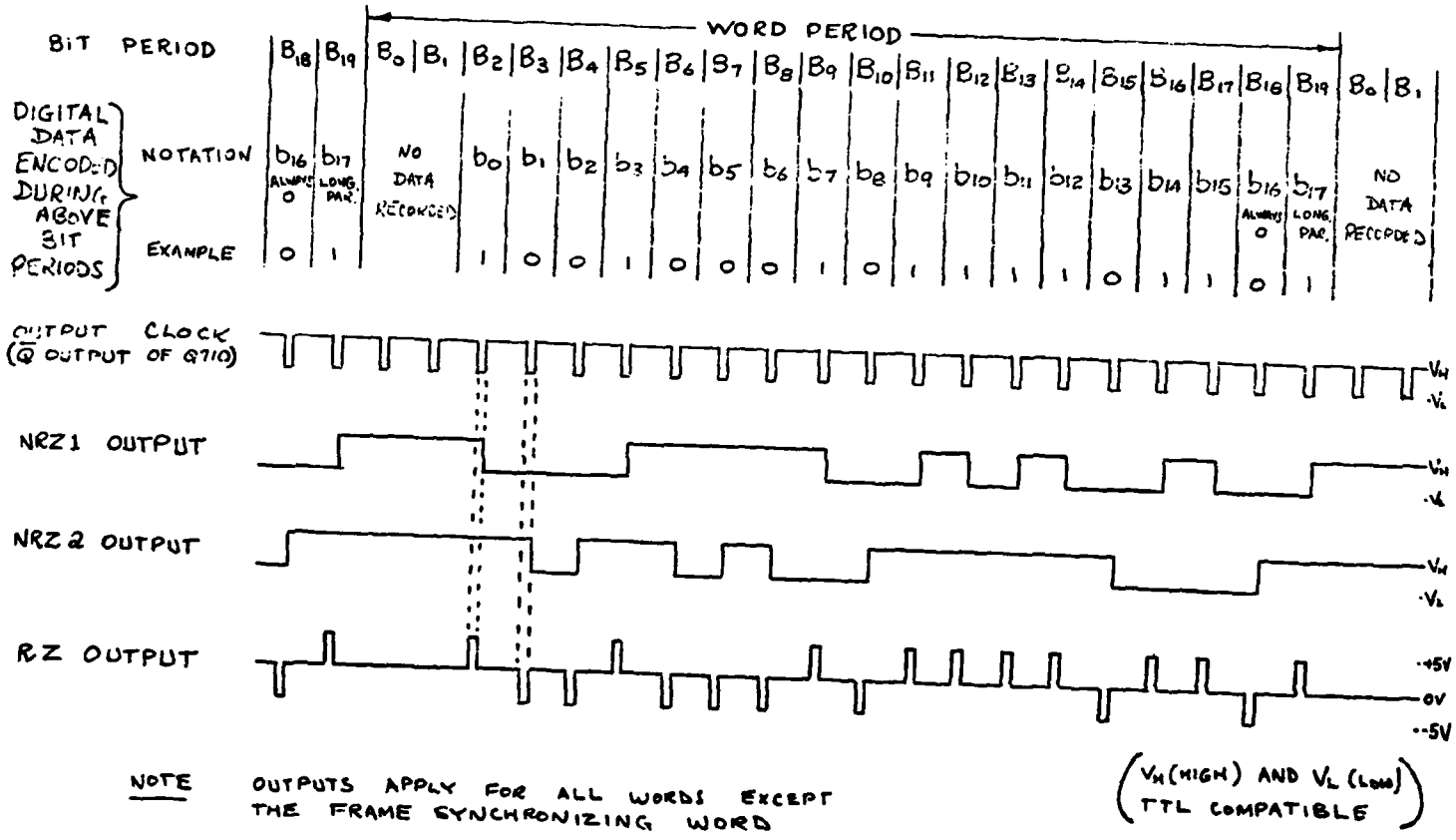


FIG. 18. OUTPUT SIGNALS FOR SERIAL SYSTEM

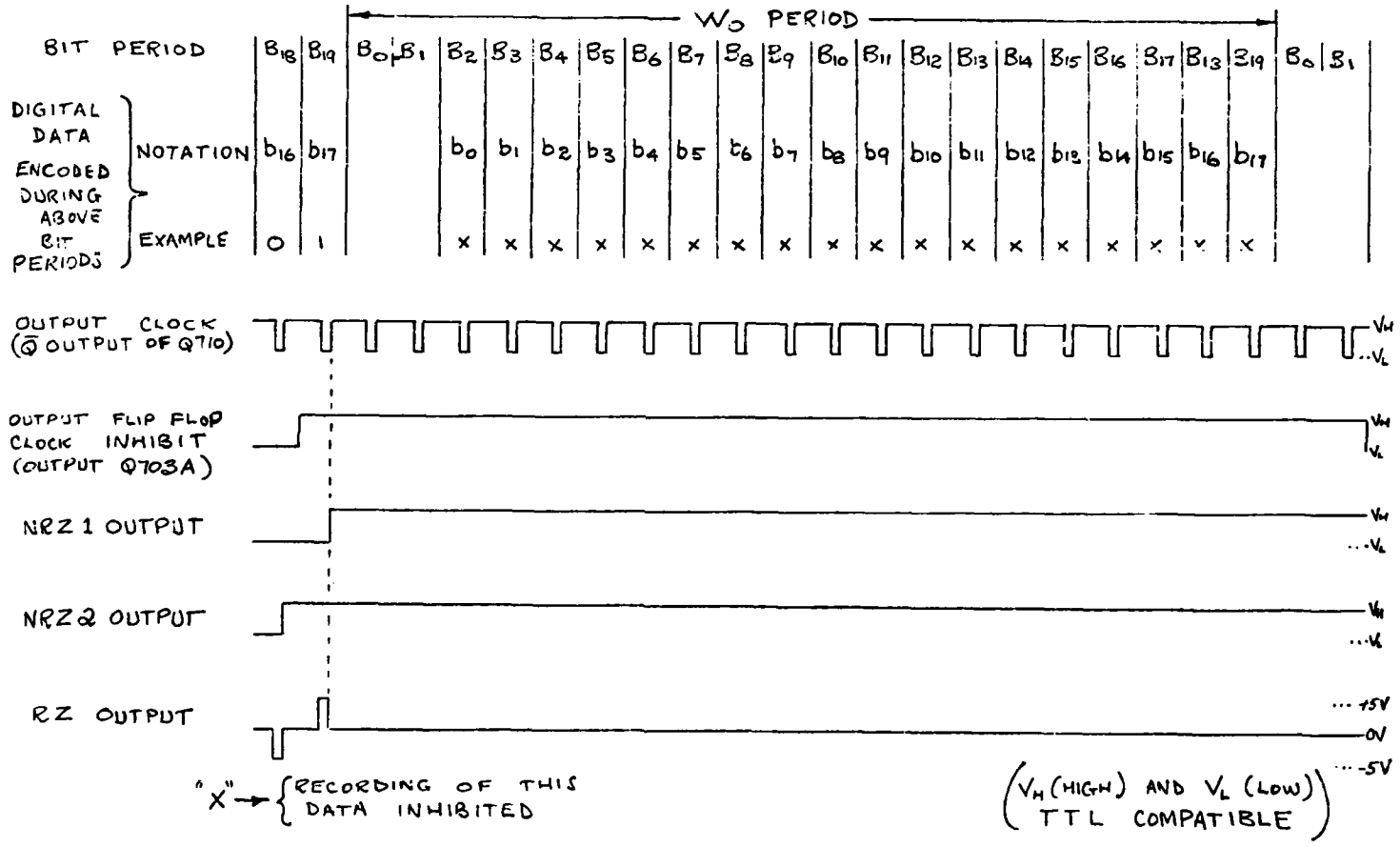


FIG. 19. FRAME SYNCHRONIZATION (TYPE A) FOR SERIAL SYSTEM)

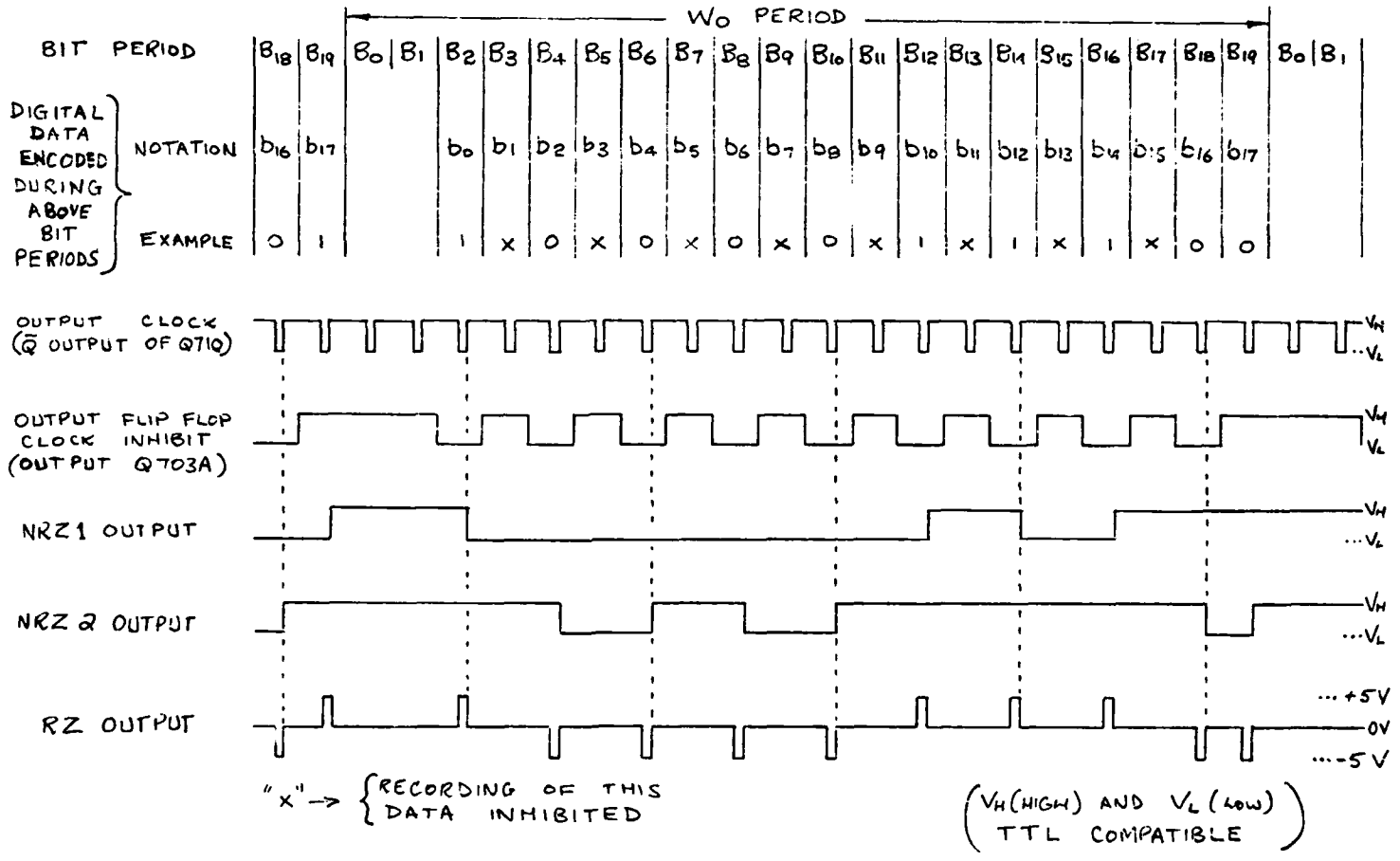


FIG. 20. FRAME SYNCHRONIZATION (TYPE B) FOR SERIAL SYSTEM

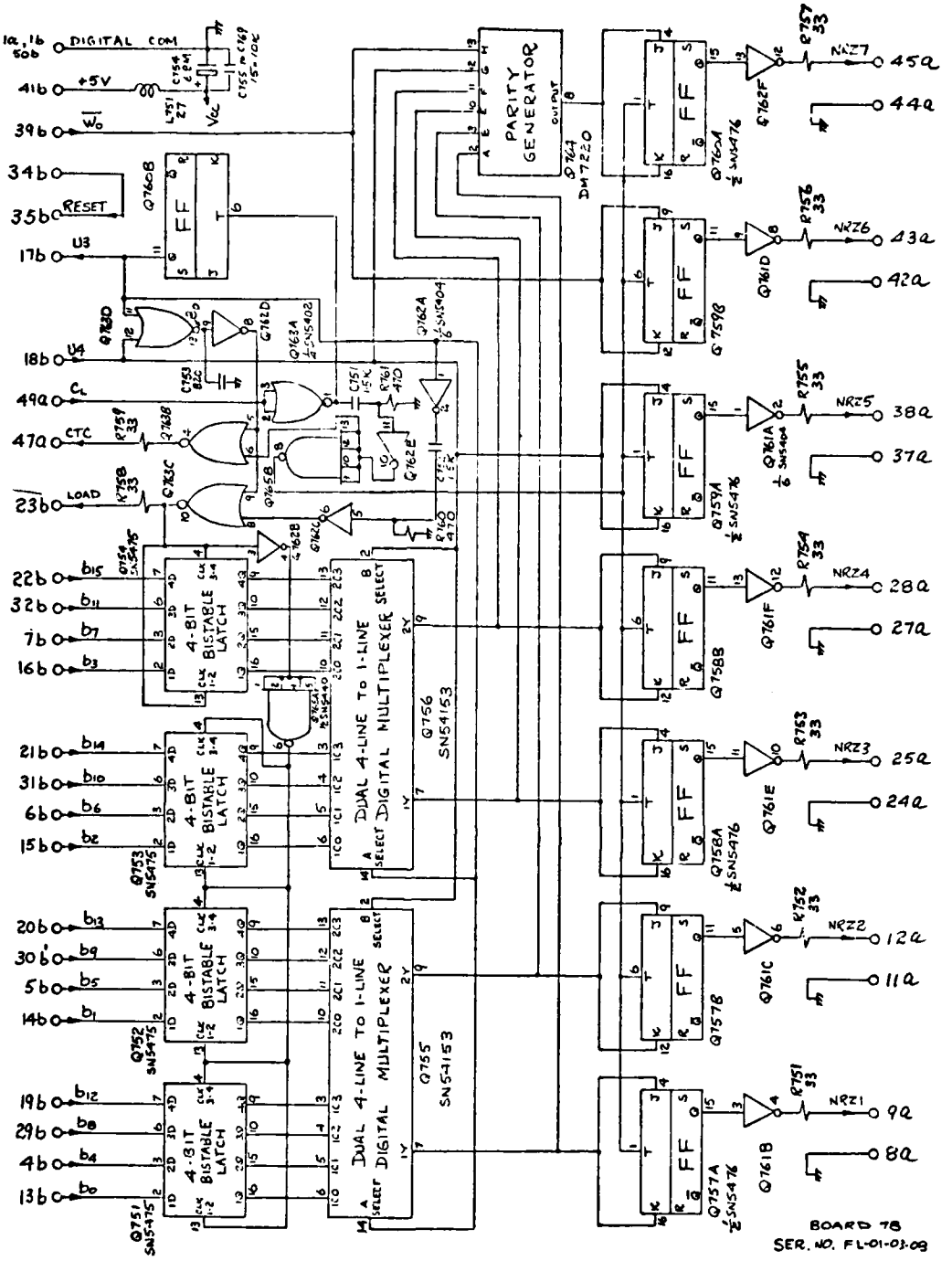


FIG. 21. PARALLEL TO SERIAL CONVERTER (parallel system)

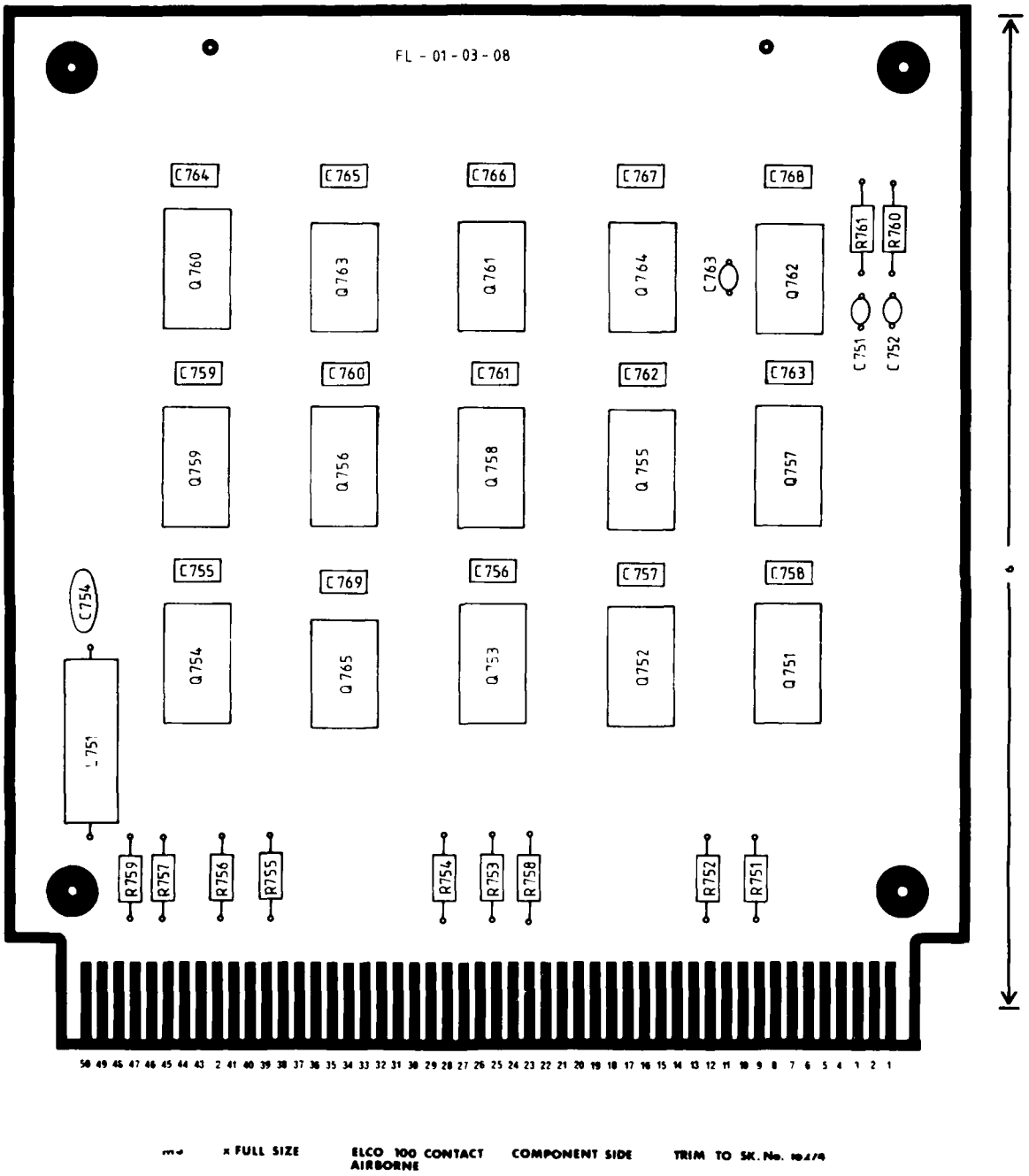


FIG. 22. COMPONENT LAYOUT FOR PARALLEL TO SERIAL CONVERTER
(parallel system)

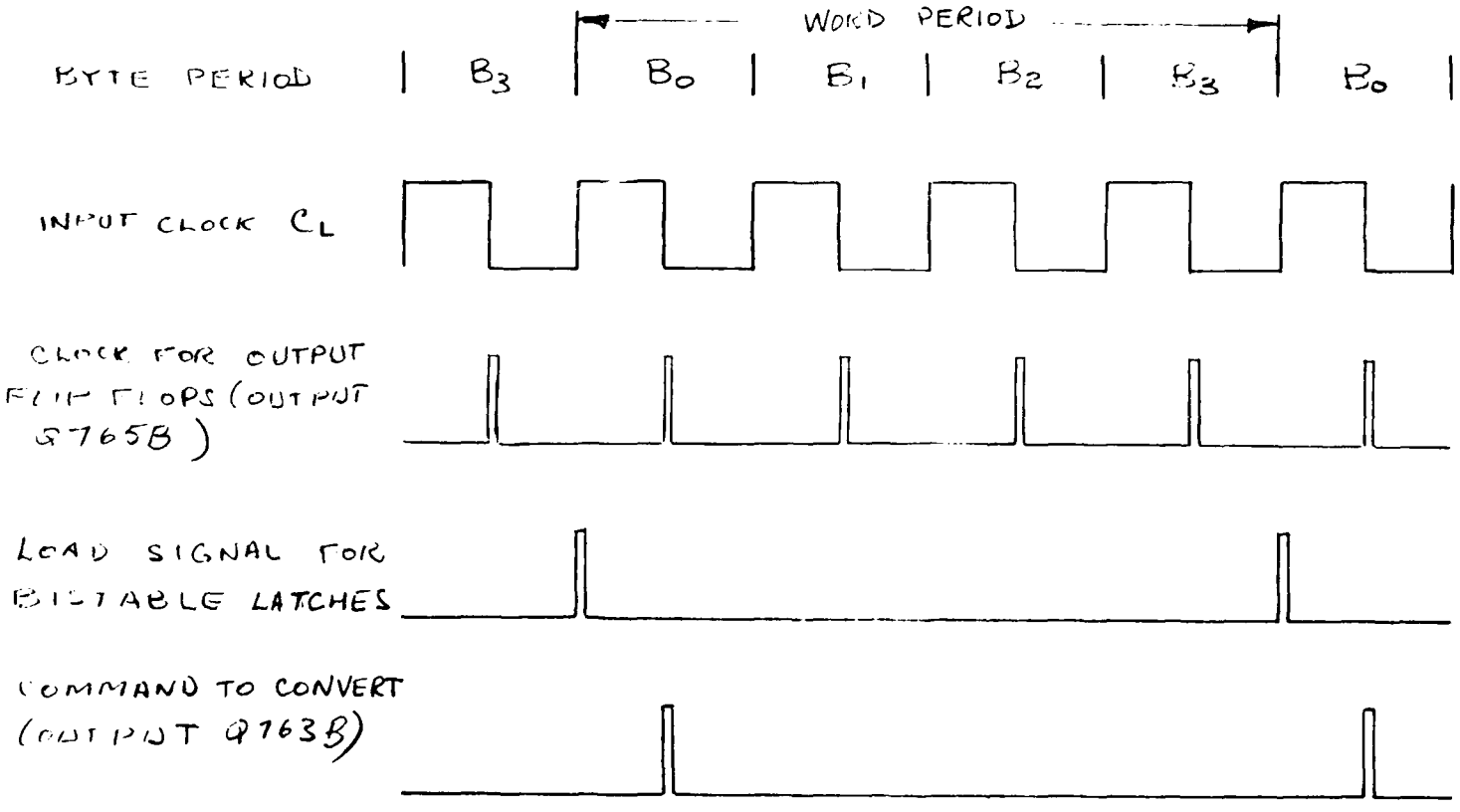


FIG. 23. CONTROL SIGNALS FOR PARALLEL TO SERIAL CONVERTER
(parallel system)

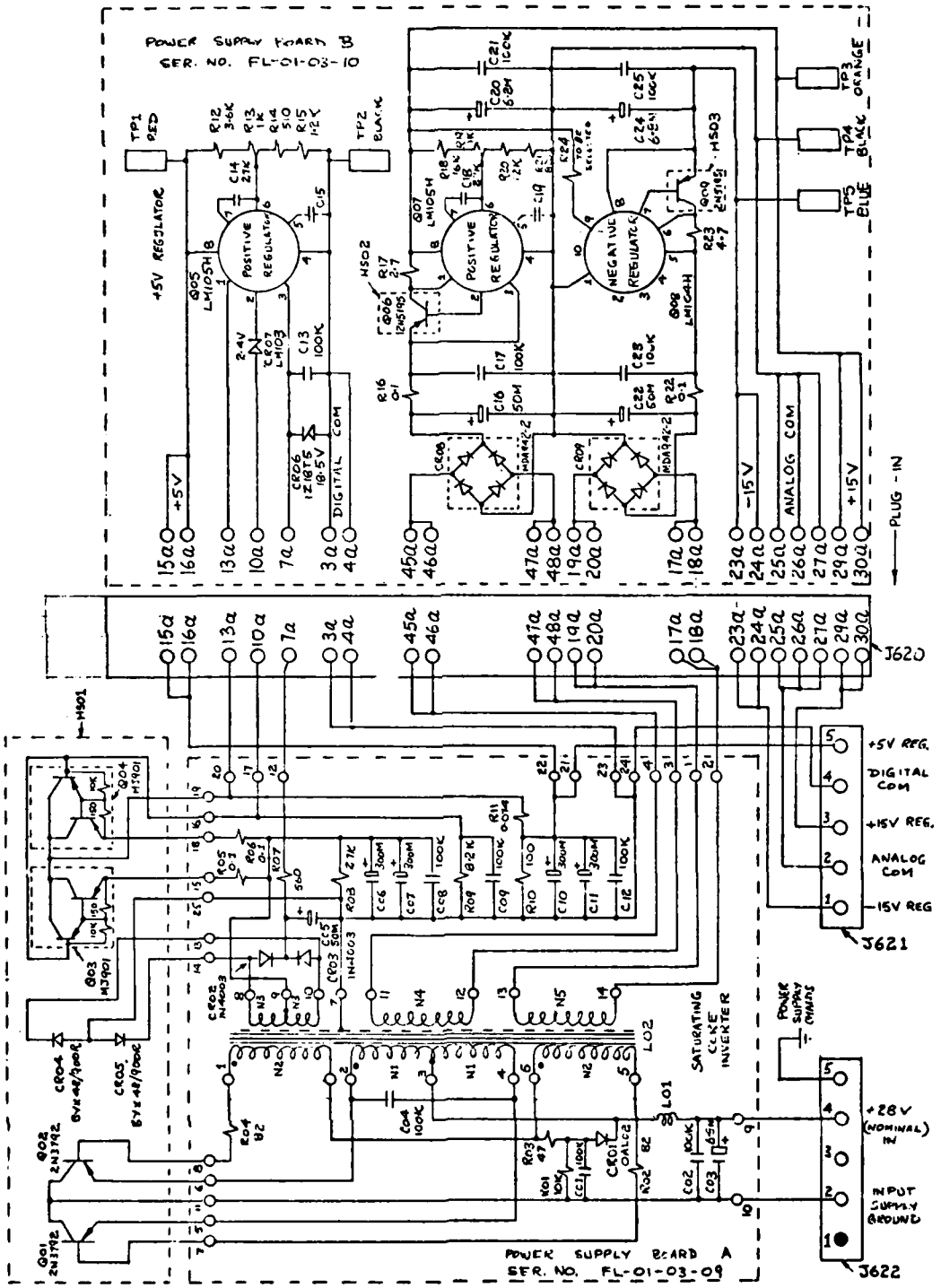


FIG. 24. POWER SUPPLY

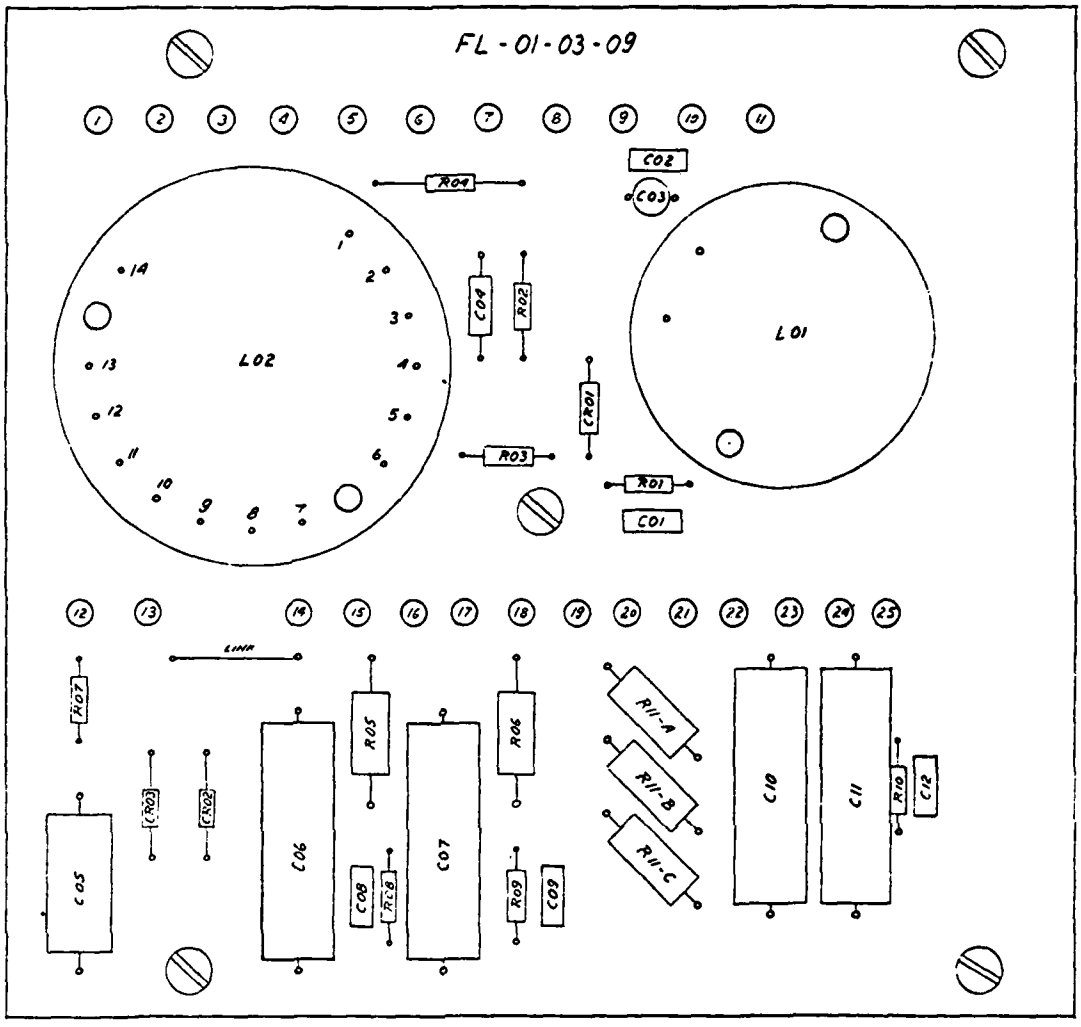
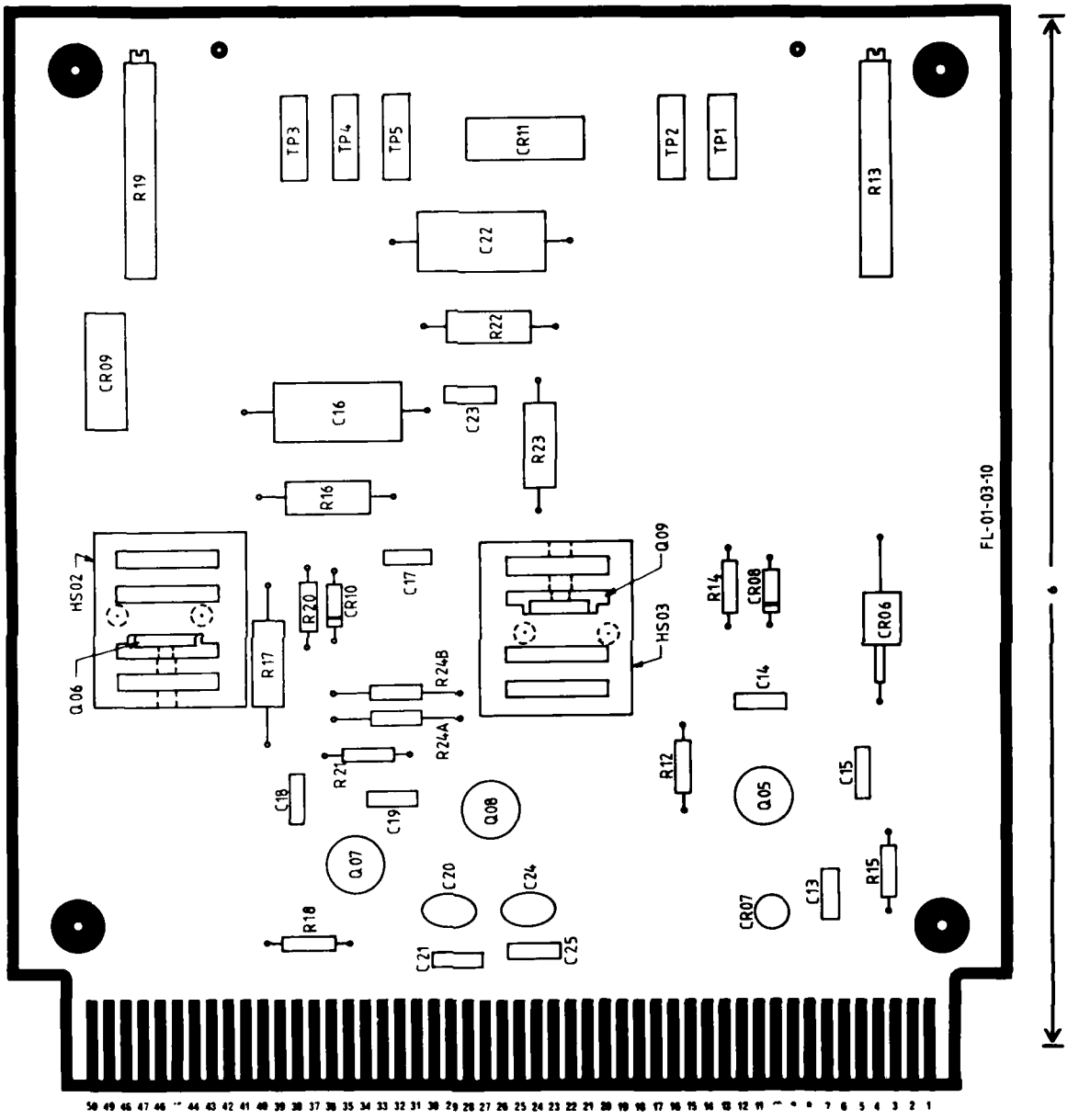


FIG. 25. COMPONENT LAYOUT FOR POWER SUPPLY BOARD A



M3 x FULL SIZE ELCO 100 CONTACT AIRBORNE COMPONENT SIDE TRIM TO SK. No. 162/4

FIG. 26. COMPONENT LAYOUT FOR POWER SUPPLY BOARD B

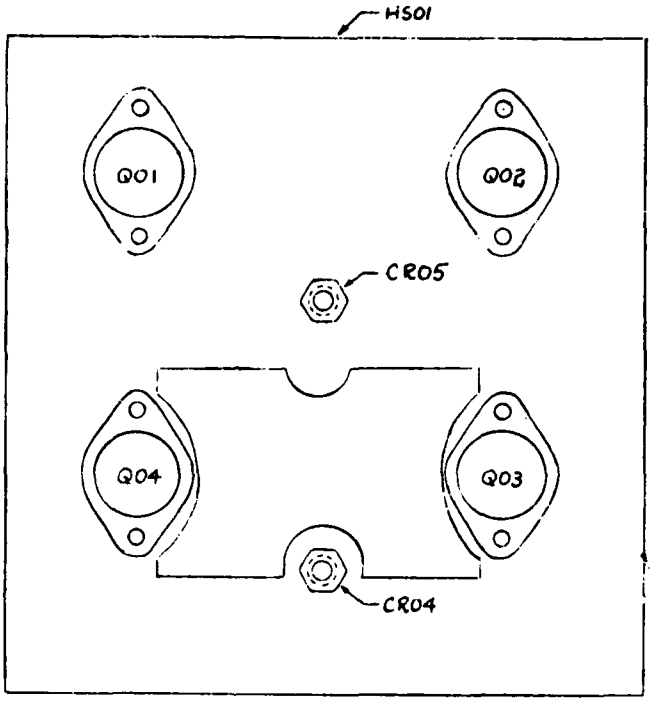


FIG. 27. COMPONENT LAYOUT FOR POWER SUPPLY HEATSINK

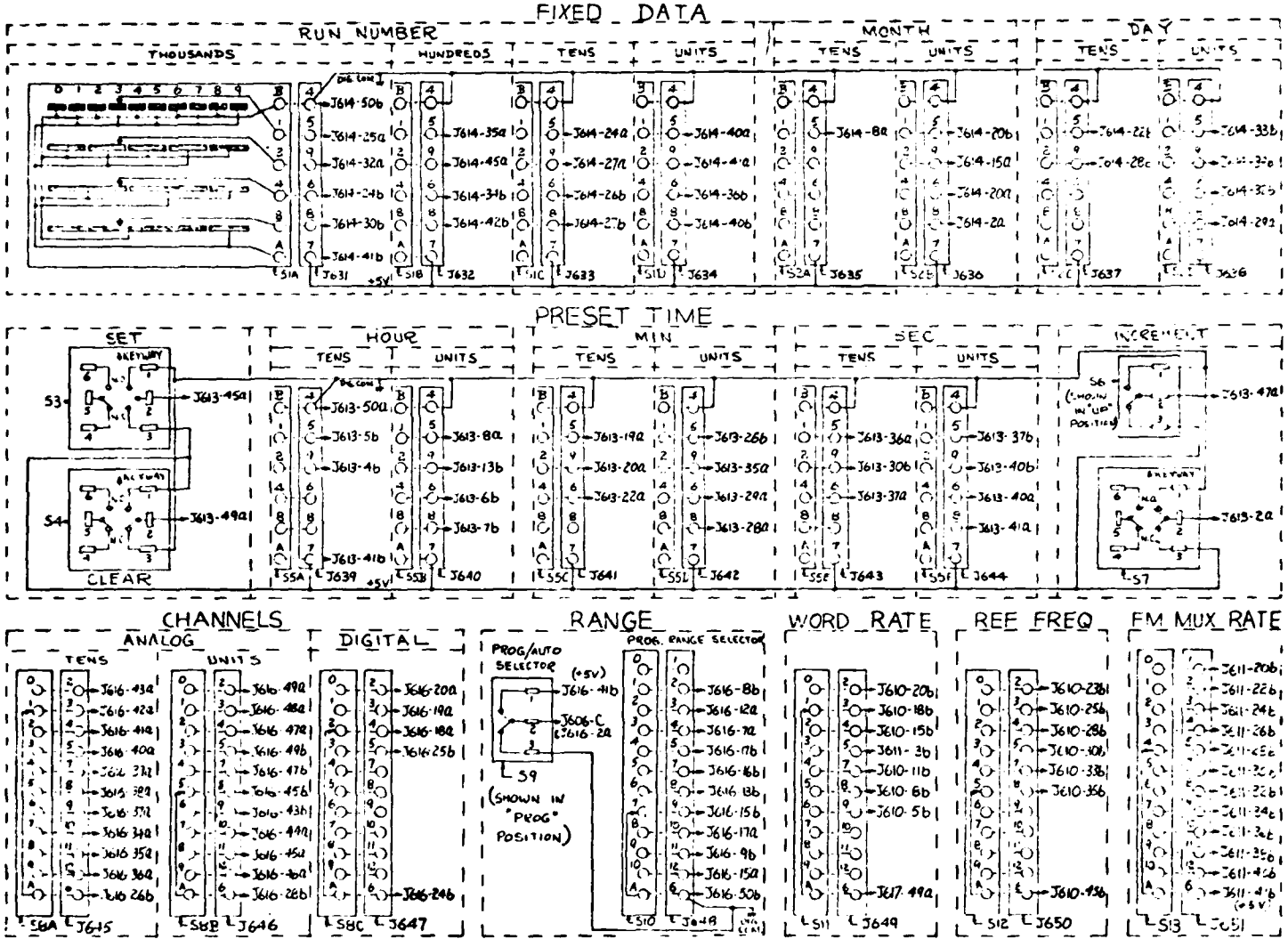


FIG. 28. WIRING DIAGRAM FOR FRONT PANEL SWITCHES

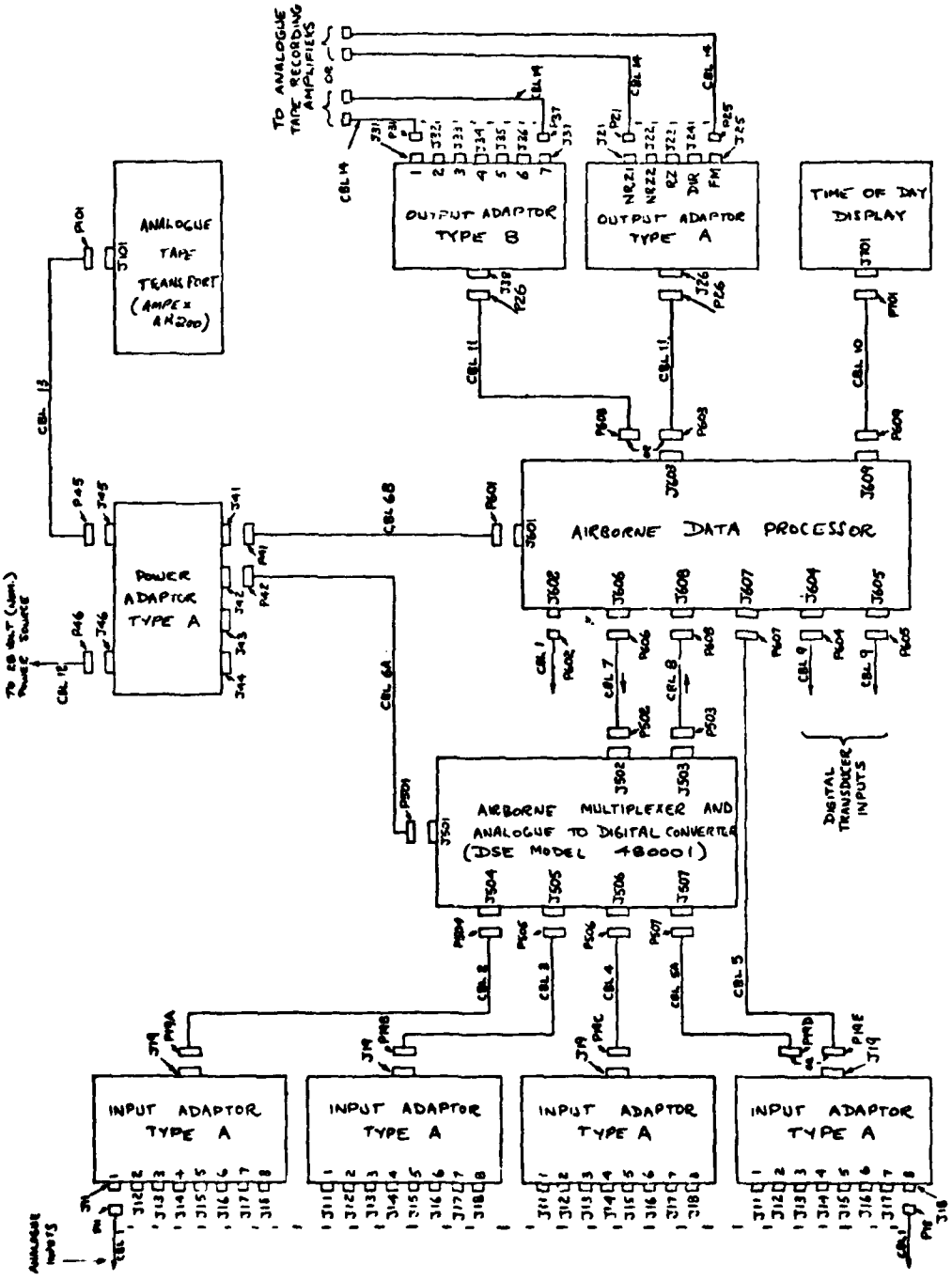


FIG. 29. CONNECTING CABLES FOR DATA PROCESSOR AND ASSOCIATED DATA ACQUISITION EQUIPMENT

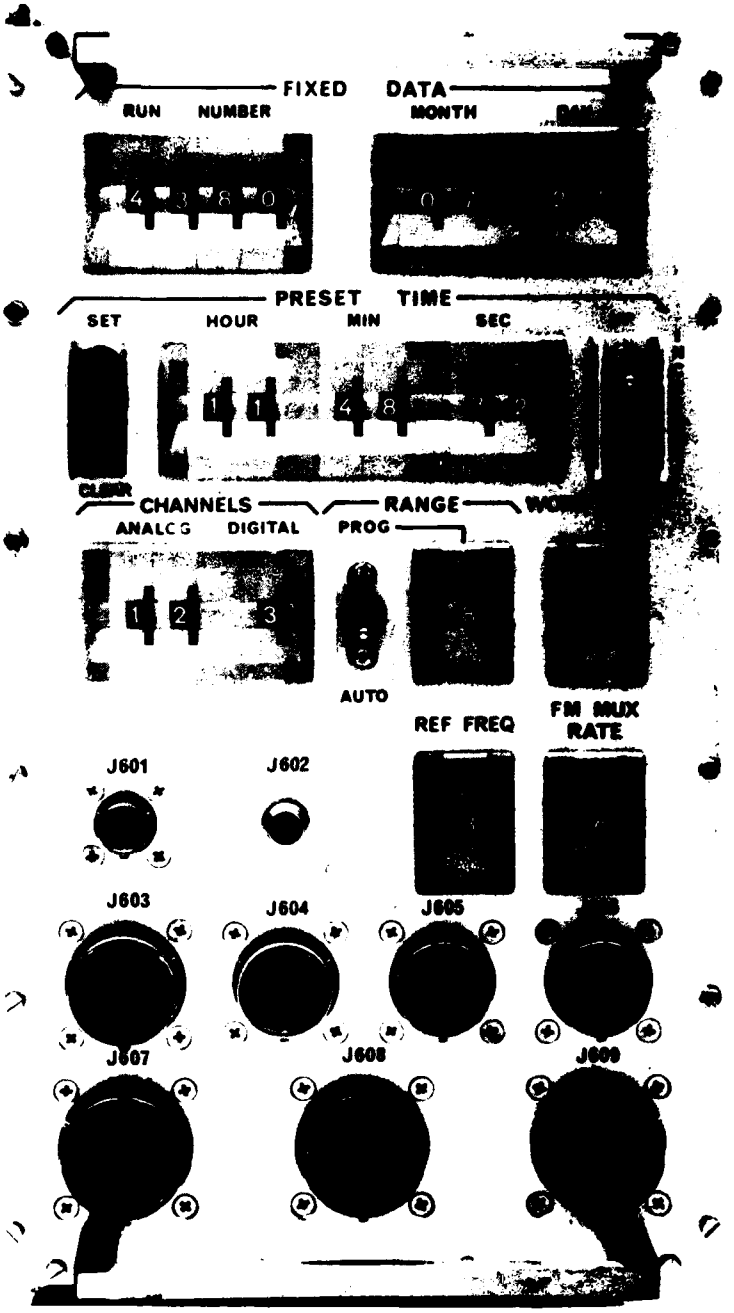


FIG. 30 (a) AIRBORNE DATA PROCESSOR – FRONT VIEW

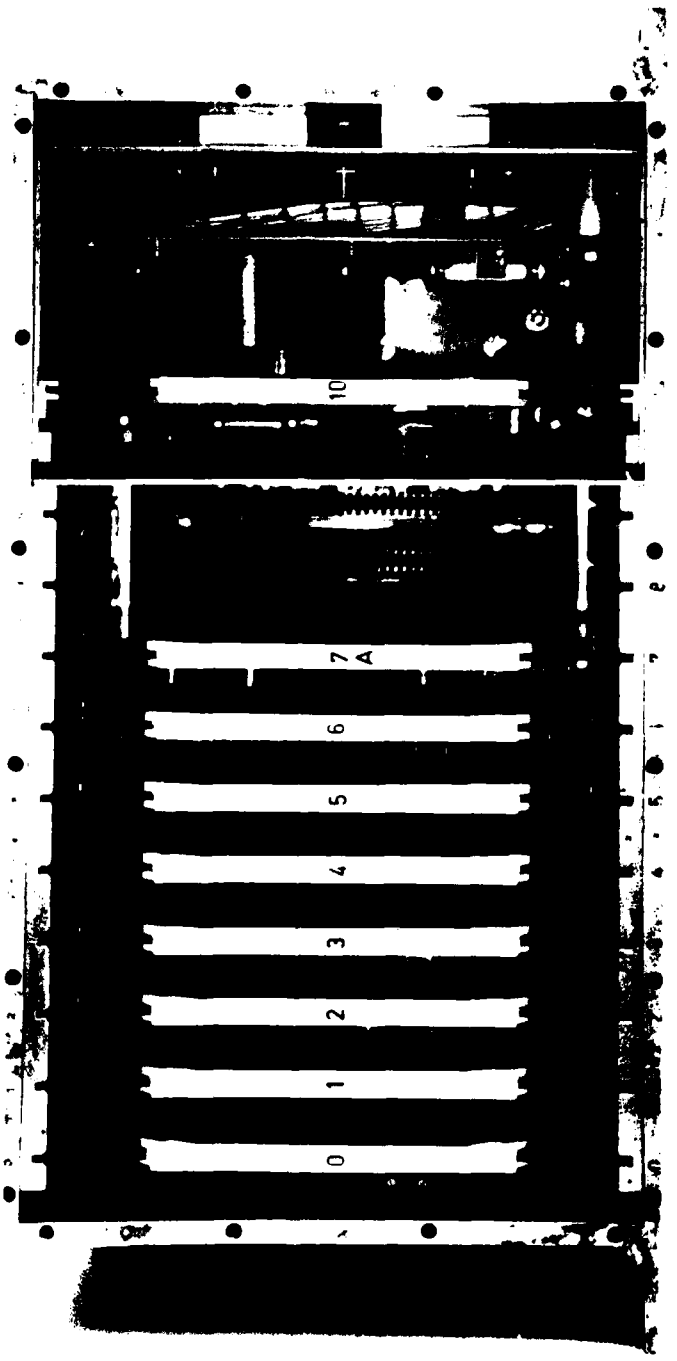


FIG. 30 (b) AIRBORNE DATA PROCESSOR – REAR VIEW

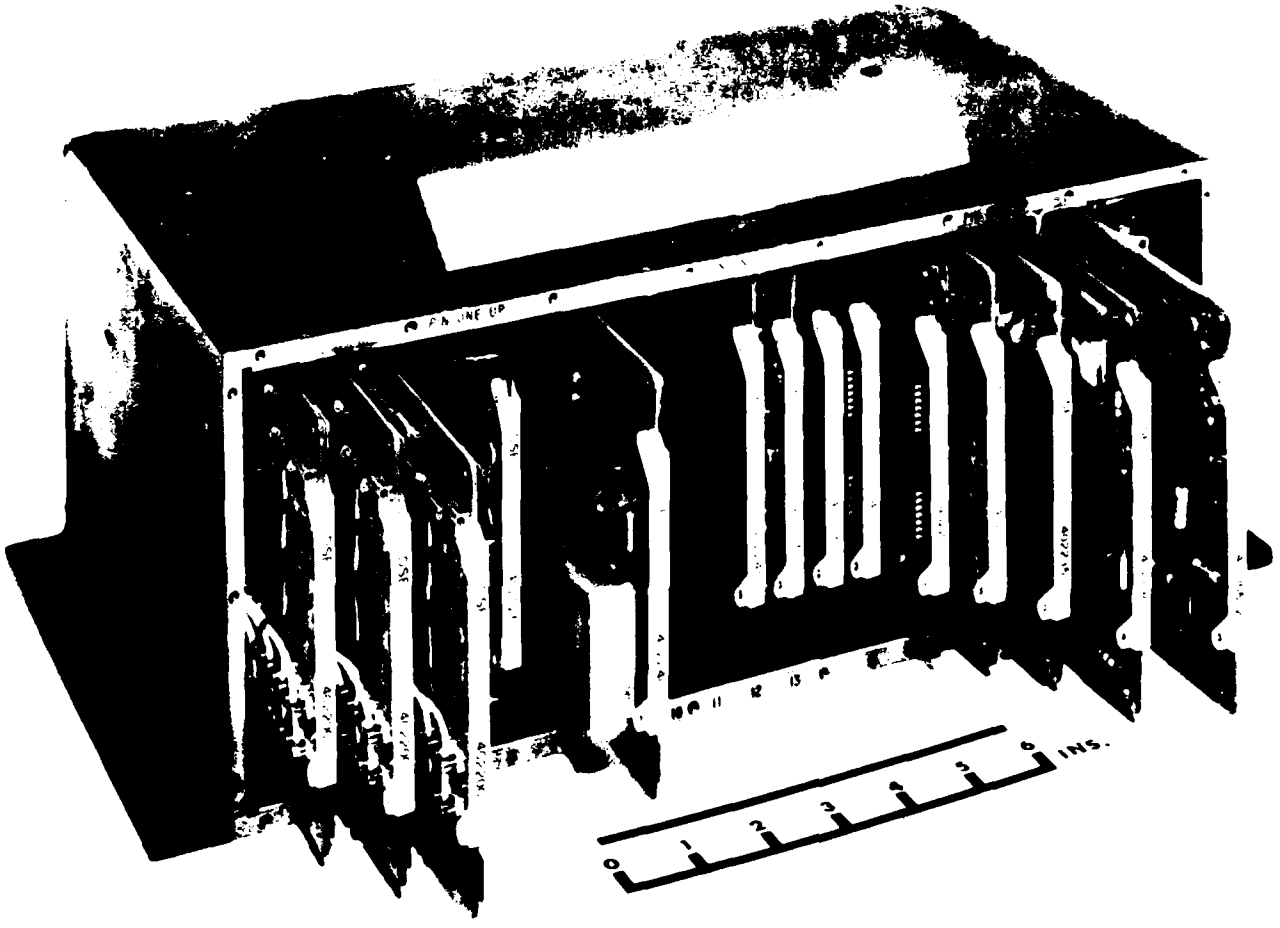


FIG. 31. AIRBORNE MULTIPLEXER AND ANALOGUE TO DIGITAL CONVERTER
(DSE Model 480001)

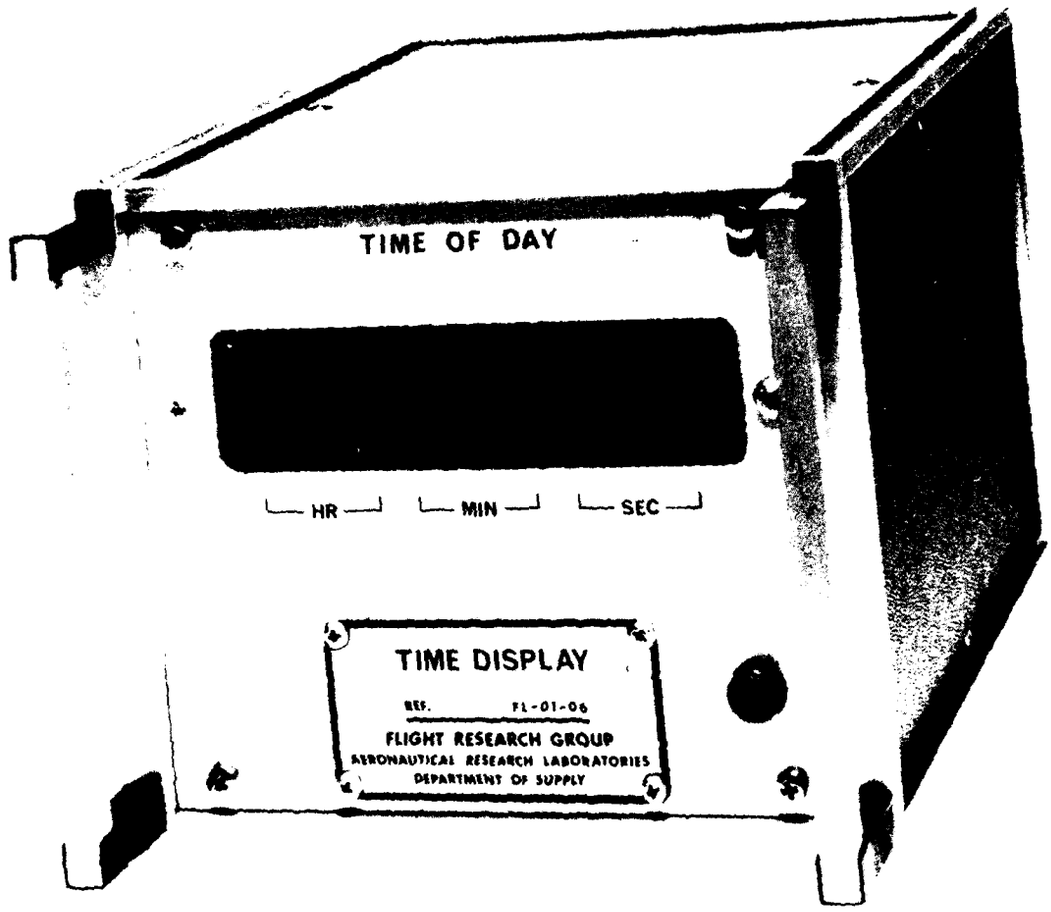


FIG. 32. TIME-OF-DAY DISPLAY

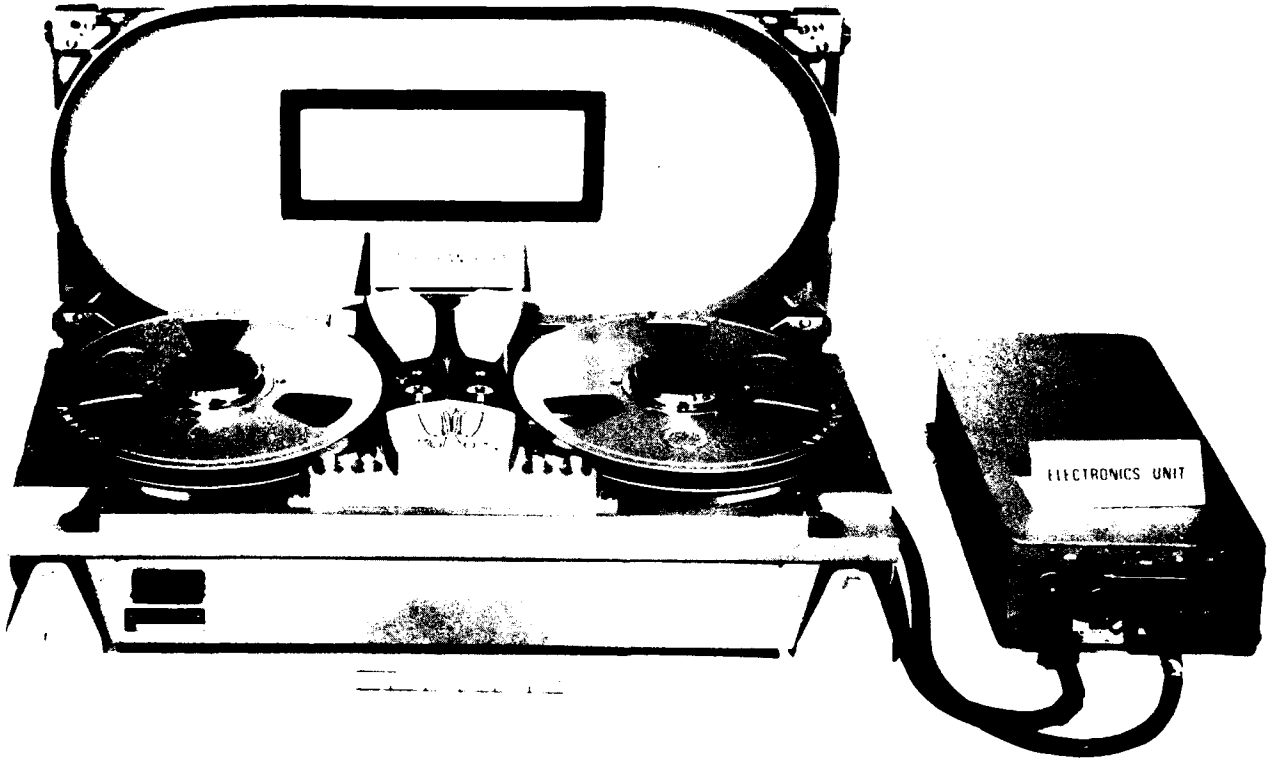


FIG. 33. TAPE RECORDING EQUIPMENT

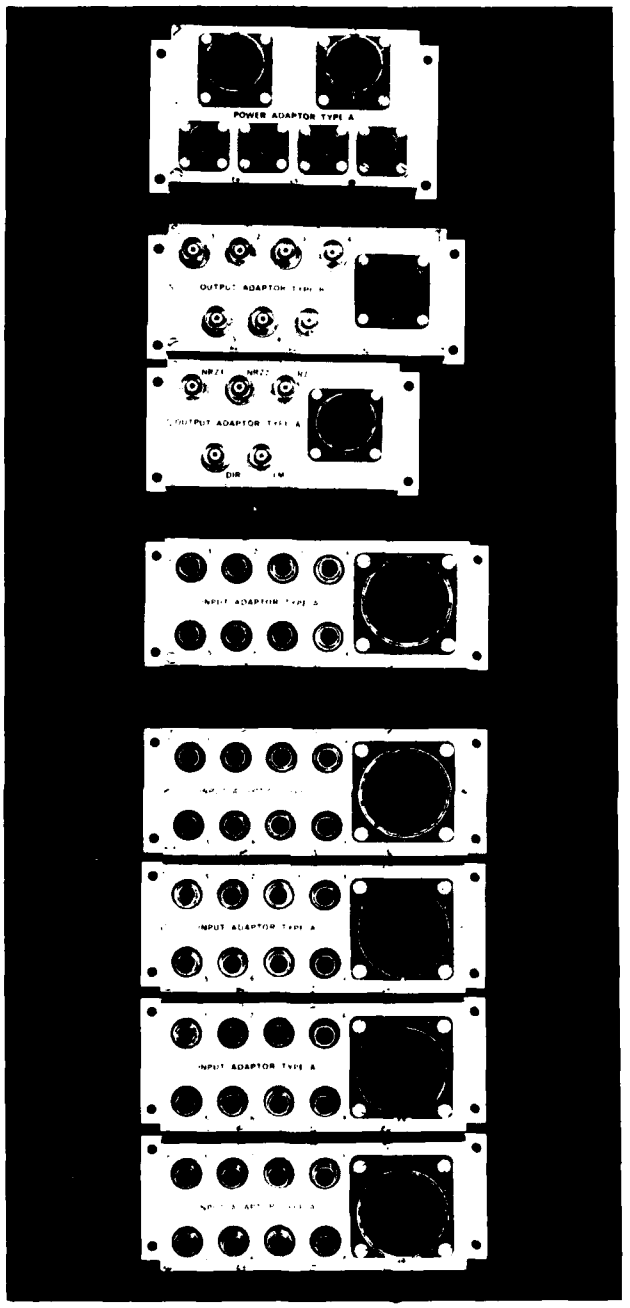
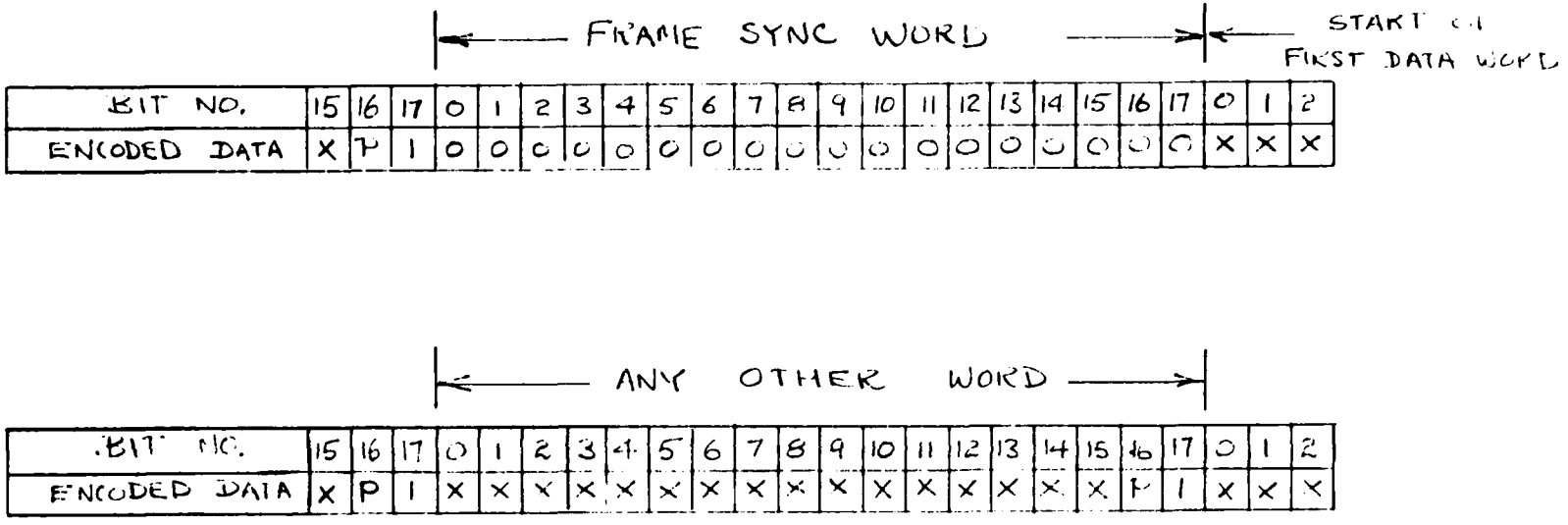


FIG. 34. CABLE ADAPTORS



"X" MAY BE "0" OR "1"

"P" IS EVEN LONGITUDINAL PARITY CHECKBIT

FIG. 35. ALTERNATIVE ENCODING SCHEME WITH NO TIME GAPS

DOCUMENT CONTROL DATA SHEET

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17.

ABSTRACT

Airborne equipment developed for use in the acquisition and recording of both analogue and digital data is described. These data are recorded using a single analogue magnetic tape transport.

A reference frequency, for use in servo speed control of the ground station tape reproducing machine, is combined with speech using a balanced modulator. Recording of these data is performed using direct techniques.

Up to eight channels of analogue data, which may require measurement over large bandwidth (up to 20 kilohertz), are time multiplexed at rates which are variable over a wide range. Recording of the multiplexed data is performed using frequency modulation techniques.

A highly stable crystal oscillator generates an input clock for a time code generator which provides time-of-day in digital form.

Up to 32 channels of analogue data, requiring measurement at relatively low bandwidth but at high accuracy, are time multiplexed and converted to digital form using commercially available airborne equipment. The digital output from the above equipment together with that from the time code generator and from up to two digital transducers are multiplexed digitally. The digital data are serialized and converted to a form suitable for recording using the analogue tape machine.

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